Stability issues in sputtered CdS/CdTe solar cells

Naba Raj Paudel

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A Dissertation

entitled

Stability Issues in Sputtered CdS/CdTe Solar Cells

by

Naba Raj Paudel

Submitted to the Graduate Faculty as partial fulfillment of the requirements for the Doctor of Philosophy Degree in Physics

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December 2011
An abstract of
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Magnetron sputtering is a well-established thin-film deposition technique which is
particularly well-suited for sub-micron layers. We use this method to deposit ultra-thin
CdS/CdTe layers on commercial transparent-conducting-oxide (TCO) coated glass and
fabricate complete solar-cell structures. Cells with CdTe thicknesses of 0.25 μm, 0.5 μm
and 0.75 μm have yielded over 8%, 11% and 12.5% efficiency respectively. With slightly
thicker CdTe, we reached 13.5% on commercial soda-lime glass (Pilkington TEC-15).
These efficiencies are possible after careful optimization of the CdCl₂ activation process
and the back contact fabrication process.

These thin-film magnetron-sputtered CdTe cells are further studied with
accelerated life testing (ALT). The ALT is performed under one-sun illumination,
without encapsulation, at 85 °C and open-circuit biasing in room ambient. We have
studied the dependence on 1) substrates with and without a high resistivity transparent
(HRT) buffer layer between the TCO and CdS, 2) CdS and CdTe thickness, 3) CdCl₂
activation parameters, and 4) Cu thickness. Among them, the Cu thickness and CdCl₂
activation are more sensitive parameters of the cell stability. The effects of CdS and CdTe thickness on stability are comparatively lower. The cell stability is independent of the substrate type; however, HRT-coated substrates produce higher cell performance when very thin CdS is used. Under this ALT (light soak at 85 °C and open circuit), any drop in efficiency is mostly dominated by $V_{OC}$ and FF loss. $J_{SC}$ is not affected unless very thin CdS or CdTe layers are used. After 900 hrs of light soaking, sputtered CdTe cells are within 5% of the original performance if they are processed with proper optimization. Under damp heat (85 °C/85% relative humidity), unencapsulated sputtered CdTe cells survived without losing any cell performance after 300 hrs of stress.

We also explored some Cu-free back contacts but found that they are not better options to improve the long-term stability of these devices over carefully optimized Cu/Au contacted cells.
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Chapter 1

Introduction to Solar Cells

1.1 Background

In the 21st century, more than 90% of energy consumption for the world is still supplied from fossil fuels and nuclear energy. The main issue of those sources is sustainability, especially with the continuous increase of the demand for energy. In addition, the choices of these energy sources have some other disadvantages as well. Nuclear energy has been thought unsafe due to some dangerous bi-products and long lasting waste problems. Fossil fuels produce CO$_2$ emissions and require costly energy expenditure to deliver the fuels. Oil, which is a major contributor of global energy consumption, Figure 1-1, has already reached close to its peak production, Figure 1-2 [1].

These days, fossil fuels are one of the biggest concerns of public health due to environmental pollution. For example, CO$_2$ emission from coal and petroleum products has indirect effects to deteriorate ozone layer and cause global warming. The rapid growth of CO$_2$ emission, Figure 1-3, has caused dramatic climate changes such as rise in earth temperature, glacier disappearance, rising global average sea level, in the past few years. According to carbon-dioxide information analysis center (CDIAC) [2], world
Figure 1-1. World marketed energy consumption by fuel type (1990-2035). The energy in y-axis is expressed in British Thermal Unit (BTU) [Note: 1 BTU = 1.055 KJ]. The projected data indicates that the energy consumption increases by 49% from 2007 to 2035. [Source: http://www.eia.gov/oiaf/ieo/International Energy Outlook 2010 retrieved on August 2011]

Figure 1-2. World annual oil production (1930-2050) measured in billion barrels per year. [Source: http://www.eia.doe.gov/oiaf/ieo/world.html, retrieved on August 2011]
Energy-related carbon dioxide emissions rose from 29.7 billion metric tons in 2007 to 33.8 billion metric tons in 2020 and 42.4 billion metric tons in 2035 - an increase of 43 percent over that period. With strong economic growth and continuous reliance on fossil fuels, much of the projected increase in carbon dioxide emissions occurs among the developing nations [2]. However, their low cost at the present time is one of the main advantages of fossil fuels in comparison to other sources.

To overcome such effects, the establishment of sustainable green energy resources is required. But finding a renewable energy which will be cheaper than fossils fuels is not an easy task. So far biomass, geothermal, wind, solar, hydroelectricity are the primary existing renewable energy sources. Except solar, the rest of the renewable options (hydro, wind, biomass, geothermal) do not have adequate global resources and are not viable due to geographical reason as well [3].

![Figure 1-3](http://cdiac.ornl.gov/trends/emis/glo.html). The rapid increase in the global CO₂ emission from 1750 to 2008. [Source: http://cdiac.ornl.gov/trends/emis/glo.html, retrieved on August 2011]
1.2 1st, 2nd and 3rd Generation of Solar Cells

In the past few decades, the development of solar cells is growing rapidly and has entered into the mainstream as a reliable source of energy. Utilizing the power of the Sun (Figure 1-4), solar cells can provide an endless supply of energy. A solar cell, also termed a photovoltaic cell, is a semiconducting device that generates electricity when light falls on it. The term “photo” means light and “voltaic” means electricity. Thus photovoltaics (PV), the direct conversion of the solar energy into electrical power is now a promising renewable, affordable, and environmentally friendly energy source.

When sunlight enters the semiconductor device the higher energy photons (actually higher than the energy gap of the semiconductor) will be absorbed and create electron-hole pairs. The movement of such electrons and holes due to the built-in field generates electricity and the physical process of converting sunlight into electricity is called the photovoltaic effect. So far various semiconductors have been identified as photovoltaic materials that can absorb most of the photons from solar spectrum (Figure 1-4) and generates the electricity. The following are some popular semiconductor materials with their corresponding energy gaps for PV applications [4].

**Table 1.1**: Semiconducting photovoltaic materials with the corresponding band gap [4].

<table>
<thead>
<tr>
<th>Semiconductor PV materials</th>
<th>Energy gap (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1.1</td>
</tr>
<tr>
<td>GaAs</td>
<td>1.42</td>
</tr>
<tr>
<td>a-Si:H</td>
<td>1.75</td>
</tr>
<tr>
<td>CdTe</td>
<td>1.5</td>
</tr>
<tr>
<td>CISe₂</td>
<td>1.0</td>
</tr>
</tbody>
</table>
The semiconductor devices discussed above are usually called conventional solar cells sometimes also called 1\textsuperscript{st} and 2\textsuperscript{nd} generation solar cells. The photo-current generation process in such devices is very simple which is due to either photon absorption for direct-band-gap materials (i.e. CdTe, GaAs, etc) or phonon-assisted absorption for indirect-band-gap materials (i.e. Si). Among these devices, Si based solar cells are highly efficient [5] and the technology has been transferred to mass production such that most of the photovoltaics industries in the world are based on Si. But this technology needs a very thick layer of Si to absorb the sunlight so that the cost of solar energy per watt is much more expensive than fossil fuels. Unlike Si, thin-film photovoltaics (CdTe, CIGS, a:Si) use very thin films to absorb the sunlight, often called 2\textsuperscript{nd} generation solar cells. In the future, the effectiveness of thin-film technology also depends on the availability of In and Te which are rare earth elements.
These days, another technology in the PV industry, often called 3rd generation solar cells, has attracted much attention of researchers. This technology basically covers a wide range of materials including organic photovoltaics, hybrid cells, dye-sensitized cells, quantum-dot solar cells, nano-materials and earth-abundant semiconductor compounds. The photo-current generation process in such devices is more complicated than conventional solar cells which might be due to various recombination issues.

Comparing with 1st and 2nd generation solar cells, much lower short-circuit current is generally realized in 3rd generation solar cells. Therefore this technology has not yet been transferred into mass production. Despite these facts, ~8.3% efficiency in a research cell has been reported for organic cells where the conventional solar cells (CIGS) have already hit > 20% efficiency in the research lab [5], Figure 1-5.

**Figure 1-5.** The best research cell efficiencies of all three generation photovoltaic devices. The graph also includes the performance of multi-junction cells and concentrator PV. [Source: [http://en.wikipedia.org/wiki/File:PVeff%28rev110901%29.jpg](http://en.wikipedia.org/wiki/File:PVeff%28rev110901%29.jpg), updated by L. Kazmerski from NREL accessed on November 2011]
1.3 Basics of Solar Cells

This section presents some basic physical processes and device parameters of solar cells that are relevant to the studies presented and discussed in later chapters.

A conventional photovoltaic cell is a p-n junction diode. When two different semiconductors (n-type & p-type) are brought together to form a metallurgical junction, electrons and holes are diffused across the junction due to the concentration gradient [6]. This interdiffusion creates a space-charge region (also called the depletion region) at the junction, Figure 1-6. It also equalizes the Fermi level of two semiconductors such that band bending occurs [4]. Because of the space-charge region, an electric field, called a built-in field \( (E_0) \), will be developed across the junction that opposes the concentration gradient so that equilibrium is set up and no further diffusion of holes and electrons occurs.

![Diagram of p-n junction](image)

**Figure 1-6.** a) The p-n junction of semiconductor diodes showing space charge region and the electric field direction, b) band diagram of p-n junction shown in Fig. a) after equalizing Fermi-level [4].
When photons are incident on these devices, photons with energy greater than the band gap of the materials will be absorbed and create electron-hole pairs. Under the influence of the built-in electric field in the depletion region, the photo-excited carriers are driven in opposite directions: electrons towards the n-type region and holes towards the p-type region. The drifted charge carriers will be collected in the external circuit with the help of additional conductors in the either side of the junction as shown in Figure 1-7. The performance of such type of solar cell can be expressed in terms of various cell parameters such as open-circuit voltage ($V_{OC}$), short-circuit current ($I_{SC}$), fill factor (FF), efficiency ($\eta$), parasitic resistances ($R_S$ and $R_{SH}$) and quantum efficiency (QE) which are explained as follows.

![Diagram of a p-n junction photovoltaic device showing current generation process due to diffusion and drifting of charge carriers](image)

**Figure 1-7.** The p-n junction photovoltaic device showing current generation process due to diffusion and drifting of charge carriers [4].
1.3.1 Open-circuit Voltage ($V_{OC}$)

When photo-excited charges accumulate near the end of semiconductor layers a “photo voltage” is introduced in the device and it reduces the built-in field. If the front and back contacts of a cell are not connected by any conductor (open-circuit), the potential difference between them is defined as the open-circuit voltage ($V_{OC}$).

Mathematically it can be defined as [4]:

$$V_{OC} = \frac{nkT}{e} \ln \left( \frac{J_L}{J_O} + 1 \right) \............................................... \ (1.1)$$

Where:
- $n$: Ideality factor
- $k$: Boltzmann constant ($1.38 \times 10^{-23} \text{ JK}^{-1}$)
- $e$: Charge of electron ($1.6 \times 10^{-19} \text{ C}$)
- $T$: Temperature (in Kelvin)
- $J_L$: Photo-generated current density (in mA/cm$^2$)
- $J_O$: Reverse saturation diode current density (in mA/cm$^2$)

The ideality factor (diode factor) is a cell parameter which characterizes the perfectness of the solar cell junction. Its value depends on the mechanisms of current transport in the junction which ultimately are controlled by the defects and impurities of the semiconductors. For example, if $n = 1$, the transport is dominated by diffusion process.
1.3.2 Short-circuit Current ($I_{SC}$)

The magnitude of the photo-generated current measured when the p-and n-sides are connected to each other with a zero-resistance external circuit, is referred as the short-circuit current, $I_{sc}$. Sometimes it is expressed as current per unit area of the solar cell which is called short-circuit current density ($J_{SC}$). The current density in the conventional solar cell can be expressed as [4]:

$$J = J_O \left( \exp \left( \frac{eV}{nkT} \right) - 1 \right) - J_L \quad \cdots \quad (1.2)$$

At short-circuit current, $V = 0$ Volts, then current density becomes $J = J_{SC} = -J_L$.

1.3.3 Fill Factor (FF)

When a finite resistance is connected in the external circuit the photo-voltage drops and the current as well. The generated power depends on the load resistance and is maximized by optimization of the load. In this case voltage and the current magnitude values are called the “maximum power” voltage, $V_{MP}$, and current, $I_{MP}$, respectively. Therefore the fill factor measures the squareness of the maximum power point of the $I$-$V$ curve in the fourth quadrant. Mathematically, it can be expressed as:

$$FF = \frac{J_{MP} \times V_{MP}}{J_{SC} \times V_{OC}} \quad \cdots \quad (1.3)$$

This equation can be further reduced into the form as [7]:

$$FF = \frac{V_{OC} - Ln(v_{OC} + 0.72)}{v_{OC} + 1} \quad \cdots \quad (1.4)$$
Where \( v_{oc} = \frac{e}{nkT} V_{oc} \) is normalized open-circuit voltage.

As shown in Figure 1-8, fill factor is the ratio of area of two rectangles formed by \( V_{MP} \) & \( J_{MP} \) and \( V_{OC} \) & \( J_{SC} \) in the fourth quadrant.

1.3.4 Efficiency (\( \eta \))

Efficiency is the most significant figure of merit of solar cell which is defined as the ratio of maximum power generated by the solar cell to the incident solar power. It can be expressed as:

\[
\eta = \frac{J_{SC} \times V_{SC} \times FF}{P_{IN}} \quad \text{............................. (1.5)}
\]

Figure 1-8. A typical dark and light J-V of CdTe based solar cell. The graph also shows the position of open-circuit voltage, short-circuit current and maximum power point.
1.3.5 Series Resistance ($R_S$) and Shunt Resistance ($R_{SH}$)

Depending upon the nature of the resistances that appear in the cell structure, the parasitic resistances can be recognized as: series resistance ($R_S$) and shunt resistance ($R_{SH}$). The series resistance arises from factors such as bulk resistance of the semiconducting layers, front contact and back contact resistance, etc. The main impact of this resistance is to reduce the fill factor of the device although excessively large values may decrease the short-circuit current. It can be estimated by taking the reciprocal of the slope of the light I-V curve at zero current (i.e. in Figure 1-8, it would be the reciprocal of the slope of the tangent drawn at $V_{OC}$). Unlike $R_S$, shunt resistance arises from some current paths caused by imperfections of the cell structure, like “pinholes”. The effect of shunt resistance in the solar cell is severe when low light is used. It also reduces the FF but the impact on $V_{OC}$ will be very small unless the device is seriously shunted. The shunt resistance can also be estimated from the reciprocal of the slope of the I-V curve at zero voltage (i.e. in Figure 1-8, it would be the reciprocal of the slope of the tangent drawn at $J_{SC}$). It is very important to know that both resistances in the solar cell structure are not necessarily ohmic. A real-world solar cell can be modeled with an equivalent circuit shown in Figure 1-9. With the introduction of $R_S$ and $R_{SH}$, Equation (1.2) can be modified as [7]:

$$J = J_O \left( \exp \left[ \frac{e(V - JR_S)}{nkT} \right] - 1 \right) + \frac{(V - JR_S)}{R_{SH}} - J_L \ldots \ldots \ldots (1.6)$$

For an ideal solar cell $R_S = 0$ and $R_{SH} = \infty$. 
1.3.6 Quantum Efficiency (QE)

The quantum efficiency of a solar cell is defined as the ratio of the number of carriers collected by a solar cell to the number of incident light photons. It actually measures the probability of generating electron-hole pairs from each incident photon. Depending on how incident photons are counted, QE is defined either as: a) external quantum efficiency (EQE) and b) internal quantum efficiency (IQE). The external quantum efficiency is the ratio of the total number of charge carriers collected to the total number of photons incident. But internal quantum efficiency does not account for the photons reflected and other absorption losses in the device structure. Therefore, the internal quantum efficiency of a solar cell always is higher than the EQE.

Figure 1-10 presents EQE of a superstrate configuration CdTe solar cell. The graph shows various optical losses; reflection and absorption from glass, absorption from bi-layer TCO (ZnO:Al/i-ZnO), absorption from a window (CdS) layer and deep penetration loss through CdTe layer. Therefore, a QE measurement is also recognized as important to understand the optical and electrical properties of the solar cell. Moreover,
QE is helpful to estimate the short-circuit current of the device which we will discuss more in Chapter 2.

![Graph showing external quantum efficiency of CdS/CdTe based thin-film solar cell.](image)

**Figure 1-10.** An external quantum efficiency of CdS/CdTe based thin-film solar cell. The device was fabricated on 1 mm thick boro-aluminosilicate glass substrate coated with ZnO:Al/i-ZnO bilayer TCO which was sputtered at UT. The graph shows different optical losses due to superstrate configuration of CdTe solar cell.

### 1.4 Thin-film Photovoltaics

Currently silicon-based solar cells are the most successful commercial photovoltaic products. Nearly 80% of the PV market is still dominated by crystalline or mono-crystalline silicon, but while competing with non-renewable energy sources it faces the problem of profitability [8]. Due to the low absorption coefficient (as shown in Figure 1-11), silicon-based modules need very thick films (~300 μm) to absorb more than 95% photons [9] that suggests an expensive manufacturing cost. Therefore thin-film technologies have entered the PV industry as potential replacements for silicon as the
primary material for fabricating cost-effective PV. Compared with Si, thin-film PV materials have higher absorption coefficients ($\alpha\sim10^5$ cm$^{-1}$) so that a couple of microns of film is enough to absorb more than 95% photons. These materials also show more than 25% theoretical efficiency, Figure 1-12, for AM1.5 spectral irradiance when a single-junction device structure is used [10]. Currently, amorphous silicon (a-Si:H), cadmium telluride (CdTe) and copper indium gallium diselenide (Cu(In,Ga)Se$_2$) are three well-established technologies in the PV industry. In the following sections, we will briefly describe the main characteristics of these three technologies as well as the future challenges.

**Figure 1-11.** Absorption coefficient of various photovoltaic materials as a function of energy band gap [9]. The graph shows a comparison of 1$^{\text{st}}$ generation (Si, GaAs), 2$^{\text{nd}}$ generation (CdTe, a-Si, CuInSe$_2$) and 3$^{\text{rd}}$ generation (MDMO-PPV, a derivative of organic semiconductor polyphenylene vinylene) PV materials.
1.4.1 Amorphous Silicon (a-Si:H)

Amorphous silicon (a-Si:H) is an inorganic thin film PV material that has an effective optical band gap of about 1.75 eV. Since the diffusion length of amorphous silicon is too low and the absorber layer is insufficient for light absorption, it uses the n-i-p structure [8]. The most common deposition technique of amorphous silicon is plasma-enhanced chemical-vapor-deposition (PECVD) with 13.56 MHz excitation [11]; however, very high frequency (70 MHz), microwave frequencies and hot-wire depositions are sometimes used for higher deposition rates. It can also be used as a top cell of double or triple-junction devices with thinner absorber layers such that higher efficiency can be realized. In such cases nano-crystalline silicon (nc-Si) and micro-
crystalline silicon (µc-Si) are commonly used as bottom cells. To date, about 12.4% efficiency in laboratory scale [12] was reported by United Solar for triple-junction device structure (a-Si:H/nc-Si:Ge/nc-Si:Ge).

The most interesting feature of the a-Si:H is the unique electronic states close to the band edge that arise from disorder and a distribution of deep states due to unpassivated dangling bonds. Due to these large number of defects in the amorphous state, the device introduces many recombination centers and reduces the cell efficiency. To overcome such effects, thin-film a-Si:H is often passivated by using gas precursors like as silane (SiH₄) or germane (GeH₄). The Stabler-Wronski effect, degradation of a-Si:H solar cells under illumination, is observed in a-Si:H cells. This effect apparently occurs under illumination due to breaking of weak/strained Si-Si bonds but can be recovered if the cells are annealed at 150 °C [8].

1.4.2 Cadmium Telluride (CdTe)

CdTe is a direct band-gap [E_g = 1.5 eV] semiconductor material which absorbs the terrestrial solar spectrum for optimal efficiency. The maximum theoretical efficiency corresponding to such a band gap is about 27% [10]. Currently, First Solar has reported a 17.3% efficiency cell [13] whereas 16.7% efficiency [12] was reported earlier by NREL for the CdTe-based laboratory scale cells. To date, several deposition techniques such as magnetron sputtering, close-spaced sublimation (CSS), vapor-transport deposition (VTD) atmospheric pressure vapor deposition (APVD), electro-deposition (ED), screen-print deposition etc. have been successfully developed for CdTe fabrication [14].
The most common superstrate configuration of the CdTe cell uses CdS \((E_g = 2.42\) eV at RT) as the heterojunction partner in the device structure. Transparent substrates (either glass or polyimides) are potential candidates for CdTe device fabrication in this configuration. To obtain high efficiency devices, polycrystalline CdTe cells need to be “activated” at elevated temperature in a chlorine/air ambient regardless of the growth method. Nevertheless the basic understanding of the process is not well understood. Moreover, selection of high work-function metals for a back contact of the CdTe cell is another challenge to fabricate an efficient and stable device. Various aspects of CdTe cells will be focused in Section 1.5.

1.4.3 Copper Indium Gallium Diselenide (CIGS)

Thin-film solar cells with an absorber layer made from \(\text{Cu(In,Ga)}\text{Se}_2\) are currently the state-of-the-art of the evolution of Cu-based chalcopyrites for use as solar cells [15]. The band gap of this ternary compound varies from 1.04-1.67 eV [16] and depends on the ratio of \(\text{Ga}/(\text{Ga+In})\). The CIGS absorber material yielding the highest efficiency (~20\%) [12] is prepared by co-evaporation from elemental sources in the substrate configuration. This process requires \(~550\) °C substrate temperature for film growth. Due to the high temperature processing, Na entered into CIGS by diffusion if a soda-lime glass substrate is used during absorber layer deposition. Later on the incorporation of Na was found to be essential for high efficiency cells partly because it reduced the resistivity of CIGS films up to two orders of magnitude [17]. But higher doses of Na lead to porous films with smaller grain size and appear to be detrimental to the cell performance. Thus optimal Na concentration is often considered to be equal to the amount of diffusion from a soda-lime glass when a micron thick Mo is used as a back contact layer [17].
1.5 **Thin-film CdTe Solar Cells (in Detail)**

Polycrystalline thin-film CdTe is currently the dominant thin-film technology in PV manufacturing. Among thin-film technologies, cadmium telluride has attracted much attention since it has a direct band gap with nearly optimal energy for terrestrial solar spectrum, high absorption coefficient, low-cost photovoltaic cells. Because of its robustness, several deposition techniques have been developed for CdTe based solar cells in laboratory scale and mass production [14]. To date, First Solar claimed 17.3% efficiency cells in laboratory scale [13] whereas Primestar claimed 12.8% efficiency for monolithic integrated CdTe module of 6687 cm$^2$ [12]. In 2001, Wu et al. from NREL has reported 16.7% efficiency [18] on CdTe solar cell. This record efficiency was held for 10 years but was topped recently by First Solar. Besides, 14% efficiency [19] has been reported for CdTe cells fabricated by magnetron sputtering, a low temperature (~250 °C) deposition method developed at University of Toledo [20].

The schematic cell stacks of a thin-film CdTe device structure in superstrate configuration is shown in Figure 1-13. In the next sections, we will briefly discuss the properties of each active layer and their impacts on cell stability.
1.5.1 TCO (Front Contact)

As shown in Figure 1-13, transparent conductive oxides (TCOs) are used for the front contacts of CdTe solar cells. For a good TCO, the material should have large optical band gap (>3eV) with >80% transmission in the visible range, very low resistivity (in the order of $10^{-4} \Omega\cdot cm$), high mobility (>30 cm$^2$V$^{-1}$S$^{-1}$) as well as low free-carrier absorption [21]. The stability of TCO is very important during high temperature cell fabrication and also in long-term basis. The typical sheet resistance of such TCOs in CdTe solar cell is about 2-15 $\Omega/\square$. To date, only n-type semiconductors have been developed commercially for front contacts of conventional solar cells. The semiconducting materials shown in Table 1.2 are the most popular TCOs for CdTe cells [21, 22].

**Figure 1-13.** Schematic cross-section view of a CdS/CdTe cell structure.
Table 1.2: The most popular TCOs for CdTe solar cell application [21, 22].

<table>
<thead>
<tr>
<th>Materials</th>
<th>Resistivity</th>
<th>Transmission</th>
<th>Stability</th>
</tr>
</thead>
<tbody>
<tr>
<td>SnO&lt;sub&gt;2&lt;/sub&gt;:F</td>
<td>(5-7)×10&lt;sup&gt;-4&lt;/sup&gt; Ω-cm</td>
<td>~80%</td>
<td>excellent</td>
</tr>
<tr>
<td>SnO&lt;sub&gt;2&lt;/sub&gt;:In&lt;sub&gt;2&lt;/sub&gt;O&lt;sub&gt;3&lt;/sub&gt;</td>
<td>2.5×10&lt;sup&gt;-4&lt;/sup&gt; Ω-cm</td>
<td>~85%</td>
<td>good</td>
</tr>
<tr>
<td>In&lt;sub&gt;2&lt;/sub&gt;O&lt;sub&gt;3&lt;/sub&gt;:F</td>
<td>2.5×10&lt;sup&gt;-4&lt;/sup&gt; Ω-cm</td>
<td>~85%</td>
<td>good</td>
</tr>
<tr>
<td>In&lt;sub&gt;2&lt;/sub&gt;O&lt;sub&gt;3&lt;/sub&gt;:GeO&lt;sub&gt;2&lt;/sub&gt;</td>
<td>2×10&lt;sup&gt;-4&lt;/sup&gt; Ω-cm</td>
<td>~85%</td>
<td>good</td>
</tr>
<tr>
<td>Cd&lt;sub&gt;2&lt;/sub&gt;SnO&lt;sub&gt;4&lt;/sub&gt;</td>
<td>2×10&lt;sup&gt;-4&lt;/sup&gt; Ω-cm</td>
<td>&gt;85%</td>
<td>fair</td>
</tr>
<tr>
<td>ZnO:Al&lt;sub&gt;2&lt;/sub&gt;O&lt;sub&gt;3&lt;/sub&gt;</td>
<td>(4-6)×10&lt;sup&gt;-4&lt;/sup&gt; Ω-cm</td>
<td>&gt;85%</td>
<td>fair</td>
</tr>
<tr>
<td>ZnO:In</td>
<td>8×10&lt;sup&gt;-4&lt;/sup&gt; Ω-cm</td>
<td>~85%</td>
<td>good</td>
</tr>
</tbody>
</table>

In the past decades, introducing a highly resistive transparent (HRT) buffer layer in between the conducting TCO and the CdS window layer was found to be advantageous in CdTe cell processing. Having a 50-100 nm thick buffer layer in the device structure allows reducing CdS thickness such that higher $J_{SC}$ can be obtained without losing $V_{OC}$ and FF [23]. In some cases, the HRT buffer layer interdiffuses with CdS yielding a thinner CdS film in the finished device and therefore improved spectral response to blue photons [24]. The typical resistivity of HRT material is about $10^{-2}$ Ω-cm. Zinc stannate (ZTO), undoped zinc oxide (ZnO), and tin oxide (SnO<sub>2</sub>) are potential candidates for the HRT buffer layers [21, 22]. Radio-frequency sputtering [19] and metal-organic-chemical-vapor-deposition (MOCVD) [25] are the most common and reliable deposition techniques for TCOs and HRT buffer layers.
1.5.2 CdS (Window Layer)

Due to limited doping concentration and high absorption coefficient, homo-junction CdTe devices are not of much interest. But n-type CdS \(E_g = 2.4\) eV is a well matched heterojunction partner for thin-film CdTe solar cells. The hexagonal wurtzite structure of CdS is a more stable phase, \(\alpha\)-CdS than zinc-blende [4] and is suitable for photovoltaic application. Several deposition techniques have been developed for CdS film deposition including rf sputtering [19], chemical bath deposition (CBD) [18], close-spaced sublimation (CSS) [26] and high vacuum evaporation (HVE) [27]. Among them CBD, sputtering and CSS are the popular techniques to deposit the hexagonal wurtzite structure. Figure 1-14 presents a plan-view image of sputtered CdS film prepared on SnO\(_2\):F coated glass substrate. The secondary electron micrograph shows about 100 nm large grains.

To improve the crystallinity of the CdS films, some different techniques were applied rather than regular crystal growth i.e. heat treatment of CdS layer prior to CdTe deposition [28], reactive sputtering of CdS in Ar\(+\)O\(_2\) or Ar\(+\)F environment followed by CdCl\(_2\) treatment in Ar + H\(_2\) ambient [26], reactive sputtering of CdS in Ar\(+\)O\(_2\) followed by heat treatment [29]. Except Romeo et al. [26], no other studies reported significant improvement in device performance and cell stability; however, the interdiffusion of CdS and TCO likely occurred due to pre-heat/CdCl\(_2\) treatment [24].

The CdS thickness is one of the important parameters of high efficiency cells. CdTe cells with thick CdS and uniformity result in stronger absorption in 400-550 nm of quantum efficiency data (Figure 1-10) and lowers the short-circuit current whereas very thin CdS (<50 nm) can create some pin-holes and results in poor fill factor and open-
circuit voltage. Therefore, an optimal CdS thickness is always required which can provide the maximum product of $J_{SC}$, $V_{OC}$ and FF. Before the selection of CdS thickness, it should be noted that about 20-30 nm CdS will be consumed during the chloride activation process of the CdS/CdTe cells [30] so that the final thickness of the window layer will be lower than for the as-grown film. On the basis of these facts, typically 70-200 nm CdS layer is normally used in CdTe solar cells.

![Secondary electron micrograph of as grown CdS film sputtered on SnO$_2$:F coated glass substrate.](image)

**Figure 1-14.** Secondary electron micrograph of as grown CdS film sputtered on SnO$_2$:F coated glass substrate.

### 1.5.3 CdTe (Absorber Layer)

Cadmium telluride is a II$^B$-VI$^A$ semiconductor material that crystallizes in the zinc-blende structure, shown in Figure 1-15. The lattice constant of CdTe is 0.6481 nm [4]. Because of high absorption coefficient, 2 μm of CdTe is thick enough to absorb more than 99% photons [14]. To this date, various deposition techniques such as; magnetron sputtering, close-spaced sublimation (CSS), vapor-transport deposition (VTD), physical
vapor deposition (PVD), metal-organic-chemical-vapor-deposition (MOCVD), electrodeposition, spray deposition and screen-print deposition are well developed for quality CdTe film production [14]. Among these growth methods, CSS film has yielded up to 16.7 % efficiency [18].

![CdTe zinc-blende structure diagram](image)

**Figure 1-15.** CdTe zinc-blende structure.

The grain morphology of CdTe films deposited at lower temperature appears remarkably different from films grown at higher substrate temperature. Smaller grains up to few hundred nanometers were observed for the sputtered films deposited at 250 °C [19] but the grain size increases significantly (> 2 μm) with vapor deposition techniques like CSS (>550 °C) [31]. Depending on the growth mode, 2-8 μm thick CdTe is normally used for solar cells. But thinning down the CdTe layer to less than 1 μm results an incomplete photon absorption as well as full depletion of the CdTe layer. The cross-section TEM image of the device structure shows a columnar growth of CdTe film as shown in Figure 1-16 [32]. The main advantage of such growth morphology is to
minimize the number of grain boundaries and voids in CdTe film which could act as recombination centers.

![TEM micrograph showing as-deposited ITO/CdS/CdTe structure. Both CdS and CdTe layers were deposited by physical vapor deposition [32].](image)

**Figure 1-16.** TEM micrograph showing as-deposited ITO/CdS/CdTe structure. Both CdS and CdTe layers were deposited by physical vapor deposition [32].

In the superstrate configuration, the CdS film is deposited before CdTe such that interdiffusion of S and Te occurs during high temperature (>400 °C) deposition. This process allows forming a CdS$_x$Te$_{1-x}$ alloy at the interface during growth which is essential for high efficiency CdTe cells. But the lower temperature growth process such as electro-deposition or sputtering does not produce interdiffusion before chloride activation.

### 1.5.4 CdCl$_2$ Treatment (Activation)

Independent of the growth process, as-grown CdTe devices exhibit poor electrical properties and yield <10% efficiency. Therefore a special heat treatment process has been realized and is routinely used in device fabrication. This popular heat treatment process is
called CdCl$_2$ activation [33]. The treatment process normally done in a chlorine and oxygen ambient at 350-450 °C, significantly improves the cell performance. In some cases the efficiency increases up to three times that of the as-grown cells [17]. The primary electronic effect of Cl incorporation in CdTe seems to be the formation of an acceptor complex with Cd vacancies ($V_{\text{CdClTe}}$) usually called the A center [34]. The CdCl$_2$ vapors and oxygen also promote grain boundary passivation and may also lead to re-crystallization of the CdTe film [35] which sometimes increases grain size by a factor of 20 if growth has done at low-temperature. Re-crystallization of CdTe also changes the grain orientation from (111) to more nearly random directions [14]. It also promotes interdiffusion of S and Te which decreases the lattice mismatch by reducing in-plane compressive stress of CdTe film [36, 37]. In addition, chloride activation significantly enhances the minority carrier lifetime in CdTe and reduces the grain-boundary recombination [38]. With the help of these mechanisms, the chloride activation increases photo-current and open-circuit voltage and significantly reduces the series resistance.

The formation of the CdS$_x$Te$_{1-x}$ alloy at the interface is the major outcome of the activation process which is essential for low-temperature growth processes. It improves the junction quality of the CdS/CdTe solar cell. The optical band gap of such alloys varies with the composition according to $E_g (x) = 2.4x + 1.51(1-x) - bx(1-x)$, with bowing parameter $b \sim 1.8$ [14] is shown in Figure 1-17. The diffusion of S into the CdTe absorber layer shifts the band gap of CdS/CdTe solar cells to longer wavelengths by a few tens of nanometers as shown in Figure 1-18. But at 500-580 nm the diffusion of Te into CdS enhances absorption and decreases the QE response.
**Figure 1-17.** Optical band gap bowing of the CdS\textsubscript{X}Te\textsubscript{1-X} alloy [14].

**Figure 1-18.** External QE of CdS/CdTe solar cells processed with two different CdS thickness and CdCl\textsubscript{2} activation time. The different in EQE at 600-825 nm is TCOs effects.
1.5.5 Metallization (Back Contact)

Due to the high electron affinity of CdTe ($\chi = 4.28$ eV), metal with a high work-function ($\Phi = \chi + E_g \approx 5.73$ eV) is needed to produce a truly ohmic back contact for CdTe cells. Except Au ($\Phi = 5.4$ eV) and Pt ($\Phi = 5.7$ eV), other metals have lower work function and will form a Schottky barrier resulting a significant limitation to hole transport from the p-type CdTe. In a circuit model, the Schottky barrier will form a diode of opposite polarity to the primary junction [39] and will decrease the cell efficiency by reducing the FF and the $V_{OC}$. Therefore, a common strategy has been used to form a highly doped $p^+$ region at the CdTe back contact in order to form a recombination junction for hole transport. According to this technique, a Te-rich layer is prepared after chloride activation and apply high carrier concentration metal as a buffer layer [17]. Then the complete device structure is subjected to annealing which diffuses buffer metal into CdTe and changes the band edge such that a quasi-ohmic contact can be produced. In the CdTe cell fabrication process, a Te-rich layer is normally prepared after chloride activation either by evaporating elemental Te [40] or applying chemical etchants such as bromine methanol (BrMeOH) or the mixture of nitric acid and phosphoric acid ($\text{HNO}_3:\text{H}_3\text{PO}_4$) [41].

Due to the high diffusivity of Cu in CdTe, Cu-based back contacts are commonly used in CdTe solar cells. The most common Cu containing contacts are: Cu/Au, Cu/graphite, Cu/Mo, Cu$_5$Te:HgTe/graphite, Cu$_5$Te/Au, ZnTe:Cu [17, 42]. Alternatively, Cu-free contacts such as Ni/Al, Au, ZnTe, Sb$_2$Te$_3$/Mo, As$_2$Te$_3$/Cu/Mo, Sb/Mo, Sb/Al are also used for CdTe cells [43, 44]. Thin-film CdTe cells fabricated with Cu, Au, Ni, Al metallization usually need a post-deposition annealing for optimal diffusion. But too
much diffusion may cause cell degradation due to the tendency of accumulation of such metals at the CdS/CdTe and CdS/TCO interfaces. Unlike Cu-based contacts, CdTe cells without intentional Cu at the back contacts have sometimes exhibited better stability; however, their initial performance is poor being limited by a non-ohmic contact [43]. More details of CdTe cell stability will be discussed in the next section.

1.5.6 Stability of CdTe Cells

The recent commercial success in thin-film CdTe photovoltaics has induced much interest in the study of long-term stability. The indoor stress conditions such as light soaking, thermal stressing, damp heat test at elevated temperature and open-circuit (OC) biasing are the most common in the laboratory scale. Because the testing conditions are accelerated, reproducible and directly correlated with the field [45-50]; however, real-world solar cells experience different temperature, humidity and biasing conditions. In these studies, the instability of the CdTe devices is attributed mostly to Cu from the back contact. Use of elemental Cu or a Cu-doped compound as the primary contact for CdTe cells, forms a low-barrier contact and enhances the initial performance. After a few hours of accelerated life testing (ALT) at 100 °C, Cu is found throughout the CdTe and CdS layers. In CdTe, Cu has been reported to exist as an interstitial ion giving rise to a shallow-donor state (Cu\textsuperscript{+}) or to substitute for a Cd atom to form an acceptor state (Cu\textsubscript{Cd}) [14, 51]. After deep diffusion, Cu accumulates in the CdS and exhibits photoconductive behavior producing a strong cross-over between light and dark IV curves [50]. Further diffusion of Cu results in voltage-dependent collection and lowers the FF and the \textit{V}_{\text{OC}} of the CdTe cells.
The most common effect usually seen in high forward bias in the current-voltage characteristics of a stressed cell is "roll-over" (see Figure 1-19) that decreases the open-circuit voltage and the FF. The back-contact deterioration can cause this effect either by forming an oxide layer with copper or reducing optimal Cu thickness due to migration [45, 51-53]. In these ALT studies, the short-circuit current ($J_{SC}$) was observed to be weakly affected. But when ALT uses testing temperature 80 °C or lower, the change in $J_{SC}$ can be observed as well [54]. Light-stressed CdTe solar cells are found to be recovered after a few days of dark rest [55]. Fisher et al. suggested that only the devices which are stressed for short period (< 20 hrs) can have reversible electronic and chemical changes such that original device performance is recovered.

Back contacts containing no Cu have been used to overcome those effects. For example Ni:P [56], HgTe [57], Sb$_2$Te$_3$/Mo or Sb/Mo [43, 48, 58] contacts have shown improved lifetimes but generally are limited by lower initial performance possibly related to the fact that doping concentration in the CdTe near the back contact is too low. Thus, Cu is a key factor for high efficiency CdTe cells but needs to be optimized for long-term stability [59, 60].

In the first study [59], we finished CdTe cells with Cu/Au contacts and tested then at 85 °C, open-circuit biasing for >1000 hrs light soaking which dropped only 5-7% in relative efficiency. The degradation was mostly due to $V_{OC}$ decrease whereas FF was remained constant over the testing period. Further discussion of this result will be added later.
Figure 1-19. Typical light J-V curve of a CdTe cell before and after 300 hrs light stressing at 85 °C and at open-circuit biasing with no encapsulation. The stressed cell shows a strong “roll-over” effect in the first quadrant.

1.6 Materials Challenges for CdTe Solar Cells

Thin films of CdS/CdTe are promising materials for photovoltaic applications for low-cost solar cells. But there are several other factors that could affect the success of manufacturability of CdTe cells. In this section we will discuss them.

High efficiency thin-film CdTe cells operate in the superstrate configuration. Therefore, glass substrates are advantageous; however, chances of utilizing some transparent polyimides cannot be neglected for low-temperature deposition. But a flexible substrate such as stainless steel is completely ruled out for CdTe cells until the substrate configuration can be made to work. In the superstrate configuration, CdS, which is the most stable heterojunction partner, is widely used in CdTe cell fabrication. Because of its high absorption coefficient ($\alpha \sim 10^5 \text{ cm}^{-1}$) and low band gap ($E_g = 2.42 \text{ eV at RT}$), only
photons of energy less than the CdS band gap are transmitted into the CdTe layers. That forces about 20% loss in short-circuit current due to 200 nm CdS layer [61].

Moreover, there are some other processing limitations which could affect the CdTe based PV industry. One of them is chloride activation process which has not been well understood yet; however, the treatment enhances grain boundary passivation and reduces the native defects density [62]. Obtaining a low resistance back-contact material is another challenge of CdTe cells which forces a bi-layer contact formation in the superstrate configuration [62]. Apart from these processing issues, there are some other factors such as; long-term reliability, science and engineering support, in-situ process diagnostics and controls, thinner absorber, high-throughput and low-cost processes, improvement in open-circuit voltage, could also affect the mass production of CdS/CdTe solar cells [63].

From material prospects, cadmium which is used in CdS, CdTe and CdCl₂ compounds, is classified as a toxin. Therefore, CdS/CdTe solar cells represent environmental hazards when worked with or disposed of at the end of their life-time [63]. On the other hand, Te is a rare material but can be extracted as a by-product of electrolytic Cu refining. But in future, if thin-film CdTe technology comes to dominate the PV market, the consumption of Te will increase dramatically so that the sufficient supply of Te for PV industry may be questionable. Therefore, new discovery of Te mines is required to sustain low-cost CdTe thin-film technology.

In this dissertation, the following chapters will discuss the results of cell performance and stability issues of sputtered CdS/CdTe cells from the materials
perspective and the fabrication process. Chapter 2 deals with the optimization of sputtered CdTe cells such that high efficiency cells for very thin absorber layers can be achieved. The optimization will be discussed for the CdS thickness, the chloride activation process, the Cu thickness and subsequent diffusion time. Chapter 3 will be about skipping of the chloride activation process. In this technique, we apply higher temperature heat treatment without any intentional chlorine and compare the results of re-crystallization, CdS$_x$Te$_{1-x}$ alloying and cell performance with the regular chloride treatments. This chapter also manifests the results of CdTe cell performance after receiving chloride treatments in various ambients i.e. nitrogen, argon and air.

In the second part of this dissertation, we present the results of accelerated life testing (ALT) of magnetron-sputtered CdS/CdTe cells. Before this, ALT has not been studied systematically on the cells grown by magnetron sputtering. Our study is limited to the open-circuit biasing condition, because that condition has been shown by other groups [50, 57] to produce larger degradation than other bias conditions. It thus allows us to obtain results more quickly using large statistical sets.

As shown in Figure 1-20(a), Hegedus, et al. [50] studied the light stress behavior (under 1.2 Sun illumination) of Cu-contacted CdTe cells at 100 °C for 10 days under several bias conditions. They found that when Cu is used as part of the back contact the short-circuit and maximum power-point biasing showed least degradation. Compared with other bias conditions, $V_{OC}$ shows the most degradation suggesting that field-driven Cu$^+$ diffusion occurs that changes the Cu$_2$Te phase into CuTe which is less conductive and decreases the FF. However, CdTe samples showed similar stability trend with dry (no etching) and wet (includes chemical etching after chloride activation) processing of
Cu, better stability was observed for later case at any biasing condition. These authors also observed the degradation on Cu-free back contacted CdTe cells. In fact the degradation of cells prepared without Cu in the back contact showed quite different degradation behavior. They did not propose a mechanism for degradation of the cells with Cu-free back contacts.

**Figure 1-20.** a) Efficiency normalized to the original data of Cu contacted CdTe cells that received light stressing at 100 °C for 10 days from Hegedus, et al. [50], and b) efficiency changes as a function of biasing condition after elevated temperature stress from Hiltner and Sites [57].
In a separate study, Hiltner & Sites [57] studied both light and dark stress effects on CdTe cells with seven different biasing conditions at 100 °C for 20 days under 1-2 sun illumination Figure 1-20(b). Unlike Hegedus, et al., cells biased at the maximum-power point were the least affected in the series. Cells at forward biasing (J>>0) resulted the poorest performance. They inferred that the cell instability was due to major loss of Cu-related acceptor states through diffusion that limits the $V_{OC}$ and FF. In such devices they also suspected accumulation of diffused Cu into CdS which finally showed photo-conductive behavior. This group also observed degradation on Cu-free back contacted (undoped graphite paste) CdTe cells but did not explain about the loss mechanism of such devices.

Further review of the data from other groups [45-55] confirms that the degradation mechanism of CdTe cells is not fully understood; however, some level of diffused Cu is measured in SIMS profile after ALT. But this measurement is insufficient to address the instability that occurs on Cu-free cells.

From Chapter 4 to Chapter 8, the dissertation is mainly focused on stability issues of sputtered CdS/CdTe cells. We search for the root causes of cell degradation after applying light soaking and damp heat tests which are important for CdTe cells and modules. In Chapter 4, the results will be discussed on the basis of highly resistive buffer layer effects and CdS thickness. Chapter 5 will discuss the impact of post-deposition processes. Chapter 6 discusses thickness-dependent stability as a function of absorber layer. In Chapter 7, we will compare the stability of our standard CdTe cells with Cu/Au contacts with cells having a Cu-free back contact i.e. Sb$_2$Te$_3$/Mo. In Chapter 8, we will introduce a high-temperature activation process called “rapid thermal processing” (RTP).
This technique allows us to treat the CdTe cells in very short period which can be more useful for industrial application. At the end, the reliability of CdTe cells after receiving RTP will be discussed. In this section, light soaking and damp heat tests results will be compared for sputtered CdTe cells. Finally, Chapter 9 summarizes the dissertation.

In this study, we use current-voltage (J-V) and quantum efficiency (QE) measurements to evaluate our CdTe cells. We also characterize thin-film samples using double beam spectrometry, x-ray diffraction (XRD), secondary electron microscopy (SEM), photoluminescence (PL), secondary ion mass spectroscopy (SIMS), four-point probe resistivity and Hall measurements. Except for SIMS, we do all these measurements at University of Toledo. SIMS data were usually taken by collaborators at the National Renewable Energy Laboratory in Golden, Colorado.
Chapter 2

Fabrication and Optimization of Ultra-thin Sputtered CdS/CdTe Cells

2.1 Introduction

In this chapter, we start with the fabrication method of sputtered CdS/CdTe solar cells that is routinely followed at University of Toledo. Our main goal is to understand the requirement of processing steps and apply their best parameters to improve the cell performance especially for ultra-thin devices (i.e. < 1 µm). But thinning the CdTe below 1 µm is more challenging due to increased shunting, incomplete photon absorption and full depletion [64]. Despite these issues, Plotnikov et al. [65] and Gupta et al. [66] have successfully fabricated ultra-thin CdTe cells that reached efficiency from 6.8-12% for 0.3-1.0 µm CdTe thickness.

Here we plan to fabricate the ultra-thin cells with appropriate optimization of deposition parameters. The optimizing variables are CdS thickness, chloride activation, Cu thickness and Cu diffusion time. With the best deposition parameters, we complete the device structure and compare the performance results with UT standard cells and with values reported by other groups.
2.2 Standard CdTe Cell Fabrication Method at University of Toledo

At the University Toledo, standard CdS/CdTe cells are normally fabricated with the following steps when commercial TCO coated soda-lime glass substrates are used.

1. **Substrate cleaning**: Glass substrates are dipped into a beaker filled with deionized (DI) water and micro-90 (50:1 ratio) [67]. The container receives 15 minutes heat treatment at 60-95 °C followed by a 30 minute ultrasonic treatment. Finally the substrates are cleaned with the help of DI water rinse and nitrogen blow.

2. **CdS deposition**: About 60-80 nm CdS is sputtered on cleaned substrates by using 4N purity target from Materion (formerly CERAC).

3. **CdTe deposition**: 2-2.3 μm CdTe is sputtered after CdS deposition by using 5N purity target from Materion. In most cases, both CdS and CdTe layers are grown inside the same chamber without breaking the vacuum (~10⁻⁷ Torr).

4. **CdCl₂ activation**: After CdS and CdTe deposition, the devices receive a few drops of a saturated solution of CdCl₂ powder (4N purity) in methanol followed by heat treatment at 387 °C for 30-35 minutes in dry (bottled) air.

5. **Back contact processing**: After a methanol rinse (no chemical etching), the treated films usually get elemental Cu (3 nm) and Au (20 nm) as back contact materials evaporated through a thin metal mask. The complete cell structures then receive 45 minutes heat treatment at 150 °C in room ambient for optimal
Cu diffusion. More than 100 dot cells are usually prepared from a 3” x 3” sample.

Hereafter, any standard fabrication method will represent these parameters unless they are specified otherwise.

Besides commercial substrates, we have the capability to grow our own TCOs such as aluminum-doped zinc oxide (AZO), indium-doped tin oxide (ITO), using sputtering. While preparing these oxide layers, we use either polyimide, aluminosilicate glass (ASG) or soda-lime glass (SLG) substrates. Both ASG and SLG substrates are 1 mm thick and ASG has slight advantage on transmission due to its low-iron content.

Our studies used Pilkington TEC glass substrates coated with SnO$_2$:F and a propriety highly resistive transparent (HRT). The glass substrates were either TEC12 ($\sim$12 $\Omega/\square$) or TEC15 ($\sim$15 $\Omega/\square$) which have different HRT thicknesses. The line of sight transmission of these substrates is shown in Figure 2-1.

2.3 Experimental

In this study, CdS/CdTe samples were sputtered in our AJA system (Figure 2-2) at 45° onto a rotating TEC15 glass substrate coated with an HRT layer. The thin films were deposited at 10 mTorr argon pressure, 50 W rf power with a substrate temperature of 270 °C. CdS layers of 35, 65, 80, 100 and 160 nm thickness were chosen for the heterojunction partner of the CdTe cells. The sputtered CdTe thicknesses were 0.25, 0.5, 0.75, 1.15, 1.65 and 2.1 µm. During deposition, the sputtering rate was calculated by using an in-situ thickness monitor system developed by Zeller et al. [68]. The final
**Figure 2-1.** Line-of-sight transmission of various substrates from Pilkington. The transmission is compared with the uncoated aluminosilicate glass.

**Figure 2-2.** CdS/CdTe sputtering system designed by AJA International located in MH3023 at the University of Toledo. [Inset shows CdTe plasma through the viewport of chamber B during sputter deposition. The CdTe deposition is occurring on the glass substrate which is face down and rotating continuously for uniform coating.]
thickness of deposited CdS/CdTe films was also verified by DEKTAK3 profilometer.

As-grown CdS/CdTe films were transferred to a homemade CdCl$_2$ activation system (Figure 2-3) for high temperature treatment. The treatment system has a glass tube furnace in which the temperature is controlled by four halogen lamps (750 Watt/lamp) 2 on the top and 2 on the bottom [69]. During activation, the CdTe samples were held between two graphite susceptors (9/16” thick) for uniform heat distribution. Two feed-through thermocouples provided temperature read-out of the susceptors. Although 387 °C has been reported as the standard activation temperature for sputtered cells [65], we treated the CdTe films at 370 °C for longer periods. The advantages of using lower temperature activation for sputtered cells will be discussed in Chapter 8.

Figure 2-3. Homemade high temperature CdCl$_2$ activation system for thin-film CdS/CdTe solar cell fabrication. The system is located in MH3021 at the University of Toledo.
After a methanol rinse, CdCl$_2$ treated samples were transferred into the bell-jar evaporation system (Figure 2-4) for Cu/Au back contact deposition. 35 dot cells of area 0.062 cm$^2$ were prepared for each CdTe thickness. The complete device structures were then annealed optimal times at 150 °C in room air ambient to diffuse Cu into CdTe. After varying all post-deposition parameters, we finally obtained the best fabrication parameters for the sputtered CdTe cells. The optimization was done on the basis of cell performance. Results are given in Table 2.1.

**Figure 2-4.** Bell-jar evaporator system for back contact processing of CdS/CdTe cells. The system is located in MH3023 at the University of Toledo.
**Table 2.1:** Optimal post-deposition processing parameters for sputtered thin-film CdTe solar cells. CdTe samples were first treated at 370 °C for chloride activation and held at 150 °C for Cu diffusion.

<table>
<thead>
<tr>
<th>CdTe thickness (µm)</th>
<th>CdCl₂ treatment time (min.)</th>
<th>Cu/Au thickness (nm)</th>
<th>Cu diffusion time (min.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.25</td>
<td>8</td>
<td>0.5/20</td>
<td>6</td>
</tr>
<tr>
<td>0.50</td>
<td>15</td>
<td>0.9/20</td>
<td>10</td>
</tr>
<tr>
<td>0.75</td>
<td>25</td>
<td>1.4/20</td>
<td>18</td>
</tr>
<tr>
<td>1.15</td>
<td>45</td>
<td>2.2/20</td>
<td>25</td>
</tr>
<tr>
<td>1.65</td>
<td>65</td>
<td>2.7/20</td>
<td>35</td>
</tr>
<tr>
<td>2.1</td>
<td>90</td>
<td>3.2/20</td>
<td>45</td>
</tr>
</tbody>
</table>

**2.4 Optimization of CdS Thickness**

One of the key factors for high efficiency CdTe cells is a well matched n-type semiconductor layer to act as a hetero-junction partner. Numerous studies have shown that CdS is the best II-VI semiconductor for CdTe cell fabrication while using the superstrate configuration (Figure 2-5). The CdTe cells with a thin HRT layer between the TCO and CdS have higher cell performance. The HRT allows us to reduce the CdS thickness to increase the transmission of blue photons into CdTe and improve the short-circuit current. But a very thick HRT shows slightly stronger absorption of red photons near 650-800 nm, as observed in Figure 2-1.

For optimization, we used standard CdTe cells with five different CdS thicknesses i.e. 35, 60, 85, 100 and 160 nm. The current-voltage characteristics of such devices are shown in Figure 2-6, where J

\[ J = \frac{22.2 \text{ mA/cm}^2}{35} \]

\[ \text{FF} = 71.0\% \]

\[ \eta = \text{Voc} = 829 \text{ mV}, Jsc = 22.2 \text{ mA/cm}^2, \text{FF} = 71.0\% \] and η =
13.1%) than other samples. This device has balanced cell parameters i.e. $V_{OC}$, $J_{SC}$ and FF such that the maximum efficiency can be achieved. On the other hand, the 35 nm CdS sample shows relatively higher $J_{SC}$ but poorer FF and $V_{OC}$ so that the overall efficiency drops under 12%. In contrast, the CdTe cell with 160 nm CdS has shown lower $J_{SC}$ due to higher absorption of blue photons but could not have any further improvement in $V_{OC}$ and FF so that efficiency again drops. Therefore, 65-100 nm CdS is discovered to be an optimum thickness range for sputtered CdTe cells when about 50 nm of HRT-coated TEC glass substrates are used. In the case of ultra-thin CdTe devices, thinner CdS layers are favorable for high efficiency cells.

![Diagram of CdS/CdTe cell structure](image.png)

**Figure 2-5.** Superstrate configuration CdS/CdTe cell structure.
Figure 2-6. Current-voltage characteristics of sputtered CdTe cells used five different CdS thicknesses. The devices were processed with UT’s standard fabrication methods.

Table 2.2: CdTe best cells performance parameters for five different CdS thicknesses. The devices were processed with UT’s standard fabrication methods.

<table>
<thead>
<tr>
<th>CdS thickness (nm)</th>
<th>Voc (mV)</th>
<th>Jsc (mA/cm²)</th>
<th>FF (%)</th>
<th>Eff (%)</th>
<th>Rs (Ω-cm²)</th>
<th>Rsh (KΩ-cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>35</td>
<td>756</td>
<td>24.1</td>
<td>60.8</td>
<td>11.0</td>
<td>6.0</td>
<td>0.7</td>
</tr>
<tr>
<td>65</td>
<td>789</td>
<td>22.9</td>
<td>67.4</td>
<td>12.2</td>
<td>4.9</td>
<td>1.1</td>
</tr>
<tr>
<td>85</td>
<td>829</td>
<td>22.2</td>
<td>71.0</td>
<td>13.1</td>
<td>4.4</td>
<td>0.9</td>
</tr>
<tr>
<td>100</td>
<td>803</td>
<td>21.5</td>
<td>68.4</td>
<td>11.8</td>
<td>4.4</td>
<td>1.2</td>
</tr>
<tr>
<td>160</td>
<td>811</td>
<td>19.7</td>
<td>69.5</td>
<td>11.1</td>
<td>5.7</td>
<td>1.6</td>
</tr>
</tbody>
</table>

It should be noted that the optimum CdS thickness we defined here is for standard sputtered (CdTe thickness = 2.1 μm) cells which may not be true for other high temperature processing methods like as close-spaced sublimation (CSS), atmospheric pressure vapor deposition (APVD) and so on. When CdTe films are grown with these
deposition techniques at 450 °C or higher temperature, S diffusion likely occurs during CdTe deposition so that the consumption of CdS increases and may require thicker CdS.

### 2.5 Optimization of CdCl$_2$ Activation

The high-temperature activation process determines the junction properties of CdS/CdTe cells when these films are grown at lower temperature. In such devices, chloride activation results in the interdiffusion of S and Te that improves the electronic properties and cell performance. Earlier studies (Plotnikov et al. [65], Gupta et al. [66]) have shown that sputtered CdTe devices are very sensitive to the CdCl$_2$ activation. For thinner cells, use of the standard treatment time results in greater interdiffusion of S and Te and ultimately reduces the cell performance. Therefore, a shorter activation time is well suited for such type of films. In this study, we chose an activation temperature of 370 °C that results in slower inter-diffusion and provides better control of this post-deposition step. At 370 °C, we applied longer treatment times as suggested by Arrhenius behavior [30], which resulted in better device efficiency and yield compared to the reported data, as will be shown later.

As mentioned before, our main goal is to fabricate high efficiency cells for < 1 μm CdTe with careful optimization of each parameter. Therefore, we chose 0.5 μm CdTe film because the effects of chloride activation and Cu thickness are clearly distinguishable on thinner samples. Figure 2-7 shows the J-V characteristic for 0.5 μm thick CdTe devices which received chloride activation at 370 °C for 3 minutes, 15 minutes, and 80 minutes. The J-V data after 3 minute treatment showed poor $V_{OC}$, $J_{SC}$ and FF, indicating that the treatment time was not enough for inter-diffusion. For the 80
minute treatment time, the device again showed lower performance. But in this case, greater inter-diffusion is expected to introduce more point defects into CdTe film, which would result in poorer electronic properties. With 15 minutes of activation time, the device exhibits the highest efficiency with noticeable improvement in $V_{OC}$ and FF. We believe that the given activation condition provided sufficient alloying of CdS$_x$Te$_{1-x}$; as a result the device shows high junction quality as well as better electrical properties than the other two devices.

![Current-voltage characteristic of CdTe cells activated for three different times at 370 °C.](image)

**Figure 2-7.** Current-voltage characteristic of 0.5 μm thick sputtered CdTe cells activated for three different times at 370 °C. CdTe cell treated for 15 minutes at 370 °C exhibited the best device performance.

In a similar way, we optimized treatment time for all six different CdTe thicknesses at 370 °C and plotted the data as presented in Table 2.1. With the best fit to optimum activation time vs. CdTe thickness (Figure 2-8), a strong correlation was found between CdCl$_2$ activation time and CdTe thickness which can be written as:
\[ t = 40 \frac{\text{min}}{\mu m} \times d \, , \quad \text{....................} \quad (2.1) \]

Where ‘\( t \)’ is the chloride activation time at 370 °C in minutes and ‘\( d \)’ is the CdTe thickness in \( \mu m \).

Figure 2-8. CdCl\(_2\) activation time vs. CdTe thickness of various CdTe cells. The cross points are observed activation time at 370 °C for highest cell efficiency and the dotted line is a straight line fitting.

2.6 Optimization of Back Contact Processing

For high efficiency devices, Cu is known to be the best dopant metal for contacting thin-film CdTe cells. But its thickness would be critical for obtaining high initial efficiency and long-term stability. Like chloride activation, sputtered cells are also known to be very sensitive to the amount of Cu at the back contact and to its diffusion time [59, 65]. Especially, when CdTe thickness is below 1 \( \mu m \), the effect of Cu increases
significantly and limits the cell performance. Here we again choose 0.5 μm CdTe cells and varied two different Cu thicknesses at the back contact. The J-V characteristic of these cells is compared in Figure 2-9. With 3 nm Cu at the back contact, an ultra-thin CdTe cell will be doped heavily (more details will be discussed on Chapter-5) and yields lower $V_{OC}$ and FF. But 0.6 nm of Cu was found to be enough to make good ohmic contact and shows an improvement in $V_{OC}$, $J_{SC}$ and FF.

Moreover, the performance of the CdTe cells also depends on the Cu diffusion time. More extensive diffusion may result in greater cell instability whereas less diffusion will lead to the “roll-over” effects due to non-ohmic contact as explained in Chapter 1, Section 1.5. Therefore we need an optimal diffusion condition such that stable devices with highest initial performance can be achieved. With these optimizations, we plot the Cu thickness and its diffusion time as a function of CdTe thickness, Figure 2-10. It can be inferred that both parameters are linearly dependent on CdTe thickness.

With these observations, we can conclude that all post-deposition parameters such as chloride activation time, Cu thickness and Cu diffusion time are critical for device performance. They linearly depend on CdTe thickness when sputter deposition is used.
Figure 2-9. Current-voltage characteristic of 0.5 μm thick sputtered CdTe cells used two different Cu thicknesses at the back contact.

Figure 2-10. Cu thickness and its diffusion time as a function of CdTe thickness. The points are observed Cu thickness (left axis) and its diffusion time (right axis) for highest cell efficiency and the dotted lines are straight line fitting. Note that the Cu diffusion was done at 150 °C in room ambient.
2.7 Champion Cells

After optimization, six different thickness CdTe cells were prepared with the parameters given in Table 2.1. The average performance of 25 CdTe cells along with the best cell performance for each thickness is shown in Table 2.3. Since shorter activation period was advantageous for thinner CdTe cells, we also choose slightly thinner CdS (~60 nm) for <1.2 \( \mu \)m CdTe cells. The cell efficiency increases as a function of CdTe thickness and almost saturates beyond 1.15 \( \mu \)m. The performance data show that CdS/CdTe cells can be fabricated with open-circuit voltages of 800 mV and fill factors over 70% with only 0.75 \( \mu \)m of CdTe, indicating excellent junction quality at this thickness and only marginal loss of short-circuit current.

**Table 2.3:** Efficiency and secondary cell performance indicators of ultra-thin CdTe cells showing the 25 cell average and the best cell. These devices completed with 60-80 nm CdS thickness and received optimal post-deposition parameters shown in Table 2.1.

<table>
<thead>
<tr>
<th>CdS/CdTe thickness (( \mu )m)</th>
<th>Solar cell performance</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( \text{V}_{\text{OC}} ) (mV)</td>
<td>( \text{J}_{\text{SC}} ) (mA/cm(^2))</td>
</tr>
<tr>
<td>0.06/0.25</td>
<td>710</td>
<td>17.5</td>
</tr>
<tr>
<td>Average</td>
<td>674</td>
<td>17.2</td>
</tr>
<tr>
<td>0.06/0.50</td>
<td>759</td>
<td>21.3</td>
</tr>
<tr>
<td>Average</td>
<td>742</td>
<td>20.4</td>
</tr>
<tr>
<td>0.06/0.75</td>
<td>800</td>
<td>22.1</td>
</tr>
<tr>
<td>Average</td>
<td>796</td>
<td>21.6</td>
</tr>
<tr>
<td>0.06/1.15</td>
<td>804</td>
<td>22.9</td>
</tr>
<tr>
<td>Average</td>
<td>788</td>
<td>22.7</td>
</tr>
<tr>
<td>0.08/1.65</td>
<td>832</td>
<td>21.4</td>
</tr>
<tr>
<td>Average</td>
<td>811</td>
<td>20.8</td>
</tr>
<tr>
<td>0.08/2.10</td>
<td>823</td>
<td>22.9</td>
</tr>
<tr>
<td>Average</td>
<td>817</td>
<td>22.6</td>
</tr>
</tbody>
</table>
Figure 2-11 shows the current-voltage characteristics of the best cells for each CdTe thickness given in Table 2.3. All J-V curves show no roll-over effects in the first quadrant indicating an excellent contact; however, ultra-thin CdTe cells use thinner Cu at the back contact.

The best efficiency for each of these CdTe thicknesses is plotted in Figure 2-12. It also shows prior work from our laboratory by Gupta, et al. [66], and by Plotnikov, et al. [65]. In addition, Figure 2-12 includes data recently reported by McCandless and Buchanan for cells prepared by vapor-transport deposition (VVTD) [70], by Jones, et al. for cell prepared by metal-organic-chemical-vapor-deposition (MOCVD) [71]. We have not included earlier data reported by Amin, et al. [72] who achieved 11.2% efficiency with 0.6 µm of CdTe on 1 mm thick borosilicate glass. It is known that 1mm borosilicate glass and high quality TCO can yield 2 mA/cm² or more of additional current and at least 10% higher efficiency. However, the use of borosilicate glass is generally considered too expensive for commercial production. Although we have achieved an outstanding performance of ultra-thin CdTe cells on standard 3.2 mm soda-lime glass and commercial SnO₂:F, there is still opportunity to improve the performance by using low iron glass with other TCO materials. The dotted line shown in Figure 2-12 is our model that will be discussed more details in Section 2.7.1.

The external quantum efficiency of various ultra-thin CdTe cells is compared with a standard cell in Figure 2-13(a) and Figure 2-13(b). For each CdTe thickness, the solid line shows the QE measured in our lab where dotted line shows the QE modeled from the absorption data of Eq. (2.2). As expected, the slope of the QE curves at 600-800 nm increases for decreasing CdTe thickness which indicates greater deep penetration loss for
Figure 2-11. Current-voltage characteristics of the best CdTe devices for various absorber layers shown in Table 2.3.

Figure 2-12. Efficiency of the best ultra-thin CdTe cells as a function of CdTe thickness. This work is shown as the solid squares, and earlier published work is from Plotnikov, et al. [65], Gupta, et al. [66], McCandless and Buchanan (VTD) [70], and Jones, et al. (MOVCD) [71]. The dashed line is from our model that uses $J_{SC}$ from the absorption data Equation (2.2).
Figure 2-13. External Quantum efficiency (EQE) of CdTe cells using two different approaches (measured and modeled with absorption data); a) for 0.25 μm and 0.5 μm, b) for 0.75 μm and 1.15 μm thick absorber layers. In both graphs, the QE of ultra-thin devices is compared with standard (2.1 μm) CdTe cell.
the thinner cells. The response of ultra-thin cells near the CdTe band edge (850 nm) does not turn on as sharply as for thicker cells which may indicate less CdS inter-diffusion, since S in the CdTe lattice lowers the band gap due to band bending in this alloy system (see Figure 1-17). The blue response of the QE data; however, indicates that all cells have a similar thickness of CdS layer remaining after activation, and considerable intermixing of CdS and CdTe near the junction. Compared with the measured data, the QE curves modeled from Eqn a 2.2 showed steeper slope at 600-800 nm. This might be attributed to partial reflection of deeply penetrated red photons from Cu/Au back contact. Such reflection can be estimated quantitatively up to 12% for 0.25 μm thick cells but decreases to 3% for 0.75 μm cells due to significant improvement in absorption.

2.7.1 Modeling the Current vs. Thickness

If one assumes that the main junction is not substantially affected by thinning the CdTe layer and that current collection is unchanged by thickness, then the primary efficiency loss should come from incomplete light absorption in the CdTe absorber layer. Thus we first determine the short-circuit current of the CdS/CdTe cells based on photo-absorption assuming 100% collection and then estimate the efficiency. The mathematical expressions for $J_{SC}$ and efficiency are given in Equations 2.2 and 2.3.

The short-circuit current density is calculated as:

$$J_{SC}(d) = \sum_{\lambda} j(\lambda)$$

$$= e \sum_{\lambda} I_o(\lambda) \times (1 - R(\lambda)) \times QE(\lambda) \times [1 - \exp(-\alpha(\lambda)d)] \quad \text{.................. (2.2)}$$
where \( I_o(\lambda) \) is the photon flux for the AM1.5 spectrum [73], \( e \) is the charge of electron, \( R(\lambda) \) is the reflection from the glass superstrate and front interfaces, \( QE(\lambda) \) is the external quantum efficiency of the best CdTe cell, \( \alpha(\lambda) \) is the absorption coefficient of CdTe, and \( d \) is the CdTe thickness. The simulated quantum efficiency by using Equation 2.2 is plotted in Figure 2-13(b). The absorption coefficient used in Equation 2.2 was derived from the extinction coefficient provided by the J.A. Woollam WVASE library, which is shown in Figure 2-14, and the reflectivity was measured in our lab. The summation over \( \lambda \) was done over 300-900 nm.

With this \( J_{SC} \) the efficiency of various thickness CdTe cells was calculated as:

\[
\eta_d = \frac{V_{OC} \times FF \times J_{SC}(d)}{P_{in}}, \quad \text{.......................................................... (2.3)}
\]

where \( V_{OC} \) and FF are the open-circuit voltage and the fill factor of the best cell for standard CdTe thickness which we obtained from J-V and \( P_{in} \) is the input power which is 100 mW/cm² for AM1.5 illumination. As expected, we obtained higher efficiency from the model which indicates comparatively lower \( V_{OC} \) and FF of thinner cells (except 0.75 \( \mu \)m) than that of standard cell.

With the help of the model expressed in Equation 2.2, we can plot the short-circuit current from three different approaches as a function of CdTe thickness, as shown in Figure 2-15. To estimate \( J_{SC} \) from QE data, we integrate the product of photon flux from AM1.5 spectrum [73] and EQE data from 300-900 wavelength range. It is likely that the short-circuit current estimated from Equation 2.2 is lower than J-V or QE measurement indicating some reflection from the back contact.
Figure 2-14. Absorption coefficient of polycrystalline CdTe films provided by J.A. Woollam WVASE library.

Figure 2-15. Short-circuit current of the best cells for each CdTe thickness obtained from three different ways; J-V (a direct measurement from the solar simulator), QE (an estimation from EQE data of the best cells for that particular thickness shown in Figure 2-13) and absorption (using from Equation 2.2).
2.8 Conclusion

Magnetron sputtered CdS/CdTe cells were fabricated with absorber layer thicknesses from 0.25 to 2.1µm. A lower activation temperature was found to be advantageous for thinner cells. Reduced Cu in the back contact and shorter diffusion times were also favorable for ultra-thin devices. The CdCl$_2$ activation time and the back contact processing parameters appear to be linearly dependent on CdTe thickness. With a careful optimization of these parameters, we were able to fabricate 8%, 11% and 12.5% efficiency cells for 0.25, 0.5 and 0.75 µm CdTe thickness, respectively. These efficiencies were achieved when the CdS layer thickness was chosen to be approximately 60 nm. In contrast, the standard 2.1 µm CdTe thickness of sputtered cells need 80 nm of CdS for the best device performance. Compared with other processing methods (i.e. VTD or MOCVD), magnetron-sputtering produces better efficiency for submicron layer thickness. These results confirm the advantages of magnetron sputtering and provide new opportunities for understanding the CdS/CdTe device operation.

The efficiency vs. CdTe thickness data follow closely a model that assumes the efficiency is limited mainly by incomplete optical absorption. With an estimation of $J_{SC}$ from absorption data, we obtained better collections from QE and J-V data which indicates partial reflection of deeply penetrated photons from the Cu/Au back contact. Thus we conclude that there are excellent opportunities for fabricating high performance, large-area CdTe cells with thickness well below 1 µm.
Chapter 3

Effects of Heat Treatment (Without CdCl₂) on the Sputtered CdTe Cells

3.1 Introduction

Grain boundaries (GBs) of thin-film polycrystalline materials are responsible for lowering the cell efficiency compared to their single crystal counterparts [74]. GBs either act as recombination centers or provide paths for diffusion of contact materials. Without proper passivation of such grain boundaries, obtaining high quality films for photovoltaic application is almost impossible. In the case of polycrystalline CdTe, the films typically need to be “activated” in CdCl₂ and air ambient at 350-450 °C [33]. With that recipe, several mechanisms such as grain growth, CdSₙTe₁₋ₙ alloying, minority carrier lifetime enhancement, GBs passivation likely occur such that significant improvement in cell performance can be realized [75]. Although the chloride activation process is almost universally used in device fabrication, the basic understanding of the role of oxygen and chlorine is poorly understood.

The main purpose of this chapter is to explore the role of temperature, chlorine, and oxygen in the fabrication process of CdTe cells. We approach this issue by starting
with CdTe films grown at relatively low temperature (sputtering), and compare the film properties and cell performance after either regular CdCl$_2$ application or high temperature heat treatment alone (no intentional CdCl$_2$ application). Here we apply a few quite different treatment conditions to the sputtered CdTe cells so that the role of temperature, chlorine and oxygen on such devices will be clearly understood. We used secondary electron microscopy (SEM), x-ray diffraction (XRD) and photoluminescence (PL) to characterize the films so that more information about interdiffusion, grain morphology and defect states can be identified.

3.2 Experimental

The CdS/CdTe films were sputtered on Pilkington's standard highly resistive layer coated TEC12 soda-lime glass substrates by using the optimal deposition conditions discussed in Section 2.2. The deposited CdS was typically 80-100 nm thick and the CdTe was 2.1-2.3 µm thick. As-grown CdS/CdTe films were then annealed for 20 minutes at 400, 425 and 450 °C in dry air. Treatment at temperatures above 450 °C introduced serious film delamination and consequently these devices were not finished. For comparison, some samples were finished with our regular CdCl$_2$ treatment condition, i.e. 30 minutes at 387 °C. All CdS/CdTe devices received our regular back contact processing, as discussed in Section 2.2.

CdS/CdTe films were characterized by SEM, XRD and PL measurements and the cell performance of the completed device structures were obtained from quantum efficiency (QE) and current-voltage (J-V) measurements.
3.3 Growth Properties and Grain Morphology

In this section, we will compare the film properties and grain morphology of heat treated (without CdCl₂) and chloride-activated CdS/CdTe films with the help of SEM, XRD and PL studies.

3.3.1 Secondary Electron Microscopy

The grain morphology of CdTe films after receiving various treatment conditions is presented in Figure 3-1. Comparing plan-view images of CdTe films, Figure 3-1(a) and 3-1(b), a clear indication of grain coalescence can be observed after a 20-minute heat treatment at 400 °C. At 450 °C, Figure 3-1(c), considerable grain growth has occurred with grains up to 2 µm in lateral dimension. The CdCl₂ treated film shows grains of similar size but with less faceting, a smoother surface and much less void structure.

![Scanning electron microscopy images of sputtered CdTe films](image)

**Figure 3-1.** Scanning electron microscopy images of sputtered CdTe films a) as grown (at 270 °C), b) annealed at 400 °C, c) annealed at 450 °C and d) standard CdCl₂ treated.
visible in plan-view image, Figure 3-1(d). A quantitative measurement of average grain size is better determined by XRD using the Debye-Scherer formula as presented in Table 3.1. The grain size increases as a function of heat treatment temperature and reveals a close agreement between SEM and XRD results (shown later).

3.3.2 X-ray Diffraction

Figure 3-2 presents the x-ray diffraction (XRD) data of the CdTe films over a wide scan from 21-80°. The data were taken at ~0.02° steps and used to find the preferred orientation of the grains. The grain orientation distribution of the polycrystalline film was analyzed from the texture coefficients [76]:

\[ C_i(hkl) = N \left[ \frac{I(hkl)}{I_o(hkl)} \right] \left[ \sum \frac{I(hkl)}{I_o(hkl)} \right]^{-1} \]  

(3.1)

where \( C_i \) is the texture coefficient for the \((h k l)\) plane, \( N \) is the number of peaks included, \( I(h k l) \) is the measured intensity of the peak \((h k l)\) and \( I_o(h k l) \) is the relative intensity of the corresponding peak from the reference powder spectrum. A peak with \( C_i >1 \) indicates a preferential orientation of grains in that direction and \( C_i = 1 \) means random orientation. As with other growth processes [36, 77, 78], our as-sputtered CdTe films show a strong preferred orientation of (111). This orientation is not affected much for 400 °C and 425 °C heat treatment but significant changes were observed on the samples annealed (without CdCl\(_2\)) at 450 °C or with regular CdCl\(_2\) activation at 387 °C, as shown in Table 3.1. With major reflections from XRD data labeled in Figure 3-2, we determined the lattice parameter 6.482-6.492 Å by applying the method developed by Taylor [79] and Nelson [80]. The difference in lattice parameter from the reference powder value of
6.481 Å indicates that the as-sputtered film has 0.17% elongation perpendicular to the growth plane and the anneal at 450 °C removes essentially all of the compressive stress producing that strain, shown in Figure 3-3. The fitted lines with larger slope than CdTe powder line indicates the greater variation of compressive stress in different direction. Compared to (111) plane, higher order planes are still showing somewhat strain.

![X-ray diffractogram of the sputtered CdS/CdTe films on HRT coated TEC12 substrate](image)

**Figure 3-2.** X-ray diffractogram of the sputtered CdS/CdTe films on HRT coated TEC12 substrate; a) as grown, b) annealed at 400 °C, c) annealed at 425 °C, d) annealed at 450 °C and e) CdCl₂ treated at 387 °C.

A narrow scan from 75-80° was performed for the CdTe samples to study intermixing of CdS and CdTe films. The peak in this region would be both (333) and (511) for random grain orientations and no strain. The doublet peak arising at 76.2° and 76.4° is from different alloy compositions at different depths in the CdS/CdTe thin film as discussed by McCandless et al. [36]. The intensity of the second peak at higher angle
Table 3.1: Texture coefficient (C_i), lattice constant (a) and grain size (L) of the CdS/CdTe films after receiving various treatment conditions.

<table>
<thead>
<tr>
<th>Treatment conditions</th>
<th>Texture coefficient (C_i)</th>
<th>Lattice constant (Å)</th>
<th>Average grain size (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(111) (220) (311) (400) (331) (422) (511)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>387 °C w/ CdCl_2</td>
<td>2.0 1.0 0.8 1.5 0.5 0.6 0.5</td>
<td>6.484</td>
<td>242</td>
</tr>
<tr>
<td>450 °C w/o CdCl_2</td>
<td>2.1 0.8 0.8 1.7 0.5 0.6 0.5</td>
<td>6.482</td>
<td>335</td>
</tr>
<tr>
<td>425 °C w/o CdCl_2</td>
<td>6.0 0.0 0.1 0.2 0.1 0.1 0.5</td>
<td>6.487</td>
<td>133</td>
</tr>
<tr>
<td>400 °C w/o CdCl_2</td>
<td>6.3 0.0 0.1 0.1 0.0 0.1 0.4</td>
<td>6.490</td>
<td>115</td>
</tr>
<tr>
<td>As grown</td>
<td>6.2 0.0 0.1 0.0 0.2 0.0 0.9</td>
<td>6.492</td>
<td>67</td>
</tr>
</tbody>
</table>

Figure 3-3. An estimation of lattice parameters of sputtered CdTe films deposited on sputtered CdS. The lattice constant is defined by using the method given by Taylor [79] and Nelson [80] for CdTe films receiving different heat treatments. The horizontal dotted line shows the lattice constants of unstrained CdTe powder.
indicates greater intermixing of S into the CdTe. In such a case, increasing S content results in a smaller lattice constant and higher diffraction angle. The data of Figure 3-4 show increasing interdiffusion of S into the CdTe as the anneal temperature is increased from 425 °C (Figure 3-3(b)) to 450 °C (Figure 3-3(c)). However, even greater interdiffusion is observed for with the CdCl₂ activated device at 387 °C (Figure 3-3(d)).

Using the Vegard relation [36], the sulfur content, ‘x’, of CdSₓTe₁₋ₓ alloy was quantitatively determined as 0.009, 0.013 and 0.017 respectively for the CdTe films that received heat treatment at 400 °C, 425 °C, 450 °C. In contrast x was 0.02 for the CdCl₂ activated sample. The analysis shows no indication of alloying (x < 0.001) in as-deposited sputtered films.

Figure 3-4. Narrow angle scan of XRD (511)/(333) profile of the sputtered CdTe films deposited on CdS/SnO₂:F substrate; a) as grown b) heat treated at 425 °C, c) heat treated at 450 °C, d) CdCl₂ treated at 387 °C.
3.3.3 Photoluminescence

The photoluminescence (PL) data taken with 488 nm laser excitation at room temperature from the junction side of CdS/CdTe films which received various treatments are compared in Figure 3-5. The most prominent PL peak located near 1.74 eV is associated with shallow defects in CdS [81]. The intensity of the peak goes up with annealing temperature and is a maximum for CdCl$_2$ treated samples, which indicates greater alloying after the chloride treatment. The red band emission near 1.63 eV is associated with phonon replicas coupled with local vibration modes in CdS [81]. The third peak located near 1.42 eV is from CdTe [14, 82] and is only significant for the samples heated to 400 °C. At higher temperatures, the peak is not appreciable due to strong alloying of CdS$_x$Te$_{1-x}$ because the penetration depth for the 488 nm laser is ~100 nm, which is equivalent to the thickness of as-deposited CdS layer (80-100 nm).

![Photoluminescence spectra of the CdS/CdTe films after annealing at three different temperatures. Data for the standard CdCl$_2$ treatment is also shown. The thin-film samples were excited on the junction side using an Argon laser (488 nm and 4.8 mW) at room temperature. [Inset shows a sketch of junction side PL set up]](image)

**Figure 3-5.** Photoluminescence spectra of the CdS/CdTe films after annealing at three different temperatures. Data for the standard CdCl$_2$ treatment is also shown. The thin-film samples were excited on the junction side using an Argon laser (488 nm and 4.8 mW) at room temperature. [Inset shows a sketch of junction side PL set up]
3.4 Cell Performance Without CdCl₂ Treatment

The results of J-V measurements performed under AM1.5 illumination on all CdTe cells are shown in Table 3.2. All device parameters; \( V_{OC} \), FF and \( J_{SC} \), are strongly affected by treatment temperature but changes in \( J_{SC} \) are the most dramatic. After receiving a 20-minute heat treatment at 450 °C in air, the best cell efficiency without CdCl₂ is reached \( \sim 11.6\% \) (\( V_{OC} = 791 \text{ mV}, J_{SC} = 20.9 \text{ mA/cm}^2 \) and FF = 69.7\%). However, these devices are still 2-3 % less efficient than the CdCl₂ treated cells. For the cells receiving heat treatment alone, we expected poor grain boundary passivation and the lower shunt resistance which was consistently observed.

Table 3.2: Performance parameters of sputtered CdS/CdTe cells after receiving various treatments. The CdTe devices annealed at 400 °C or higher temperatures were treated without CdCl₂.

<table>
<thead>
<tr>
<th>Treatment conditions</th>
<th>( V_{OC} ) (mV)</th>
<th>( J_{SC} ) (mA/cm²)</th>
<th>FF (%)</th>
<th>Eff (%)</th>
<th>( R_S ) (( \Omega )-cm²)</th>
<th>( R_{SH} ) (K( \Omega )-cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>400 °C w/o CdCl₂</td>
<td>Best</td>
<td>690</td>
<td>13.9</td>
<td>55.9</td>
<td>5.3</td>
<td>10.5</td>
</tr>
<tr>
<td></td>
<td>Average</td>
<td>642</td>
<td>8.5</td>
<td>52.4</td>
<td>2.9</td>
<td>19.7</td>
</tr>
<tr>
<td>425 °C w/o CdCl₂</td>
<td>Best</td>
<td>715</td>
<td>19.1</td>
<td>58.6</td>
<td>7.9</td>
<td>7.4</td>
</tr>
<tr>
<td></td>
<td>Average</td>
<td>696</td>
<td>15.7</td>
<td>55.2</td>
<td>6.1</td>
<td>9.4</td>
</tr>
<tr>
<td>450 °C w/o CdCl₂</td>
<td>Best</td>
<td>791</td>
<td>20.9</td>
<td>69.7</td>
<td>11.6</td>
<td>4.8</td>
</tr>
<tr>
<td></td>
<td>Average</td>
<td>767</td>
<td>19.4</td>
<td>66.3</td>
<td>9.9</td>
<td>8.1</td>
</tr>
<tr>
<td>387 °C w/ CdCl₂</td>
<td>Best</td>
<td>839</td>
<td>22.5</td>
<td>71.2</td>
<td>13.4</td>
<td>5.3</td>
</tr>
<tr>
<td></td>
<td>Average</td>
<td>820</td>
<td>22.5</td>
<td>68.5</td>
<td>12.7</td>
<td>5.7</td>
</tr>
</tbody>
</table>

The current-voltage characteristics of the CdTe cells treated without CdCl₂ are compared with our regular CdCl₂ treated cells in Figure 3-6(a). As described above, the sputtered CdTe cells improve their performances with treatment temperature which is
largest for short-circuit current; however, an enhancement in open-circuit voltage and fill factor is also observed. The CdTe devices show better crystallinity that improves the electrical properties of the films and increases the cell performance. CdTe films also show greater interdiffusion of S and Te with heat treatment temperature that improves the junction quality as well.

Quantum efficiency measurements (Figure 3-6(b)) of the cells presented in Figure 3-6(a) show a substantial improvement in red photon collection when a device receives heat treatment at 425 °C. The device shows still better deep-penetration collection when the treatment temperature reaches 450 °C and even slightly better with CdCl₂ activation at 387 °C. The greater S diffusion into CdTe shifts the absorption edge slightly to longer wavelengths (830-850 nm) and also improves the response at 450 nm which is directly due to a reduction in CdS thickness.

The QE of regular chloride treated sample shows better alloying at CdS/CdTe interface as well as the better passivation of grain boundaries than any heat treated samples which is consistent with SEM and XRD results as presented in Figure 3-1 and Figure 3-4.

3.5 Cell Performance With Subsequent CdCl₂ Treatment

In this section, we will analyze the cell performance results of sputtered CdTe cells after applying a two-step post deposition treatment. CdTe films first received a 20-minute heat treatment (without CdCl₂) at 400 °C, 425 °C and 450 °C followed by a 5-minute CdCl₂ treatment at 400 °C. The ultimate goal of follow-up treatment is to
introduce chlorine in CdTe films and observe its impact on the cell performance for all annealed cells.

**Figure 3-6.** Performance of sputtered CdS/CdTe solar cells after receiving different treatments in air ambient; a) J-V characteristics of the best cells and b) external quantum efficiencies of the cells shown in Figure 3-6(a).
With subsequent chloride activation, the performance parameters increased. The effect was substantial on $V_{OC}$, $J_{SC}$, FF and hence the efficiency for the samples which had received heat treatment (without CdCl$_2$) at 400 °C and 425 °C shown in Figure 3-7. Our understanding is that the short CdCl$_2$ activation completed crystal regrowth with better alloying and passivated the grain boundaries leading to improved performance parameters. On the other hand, CdTe cells which received heat treatment (without CdCl$_2$) at 450 °C did not show improvement in cell efficiency with an additional CdCl$_2$ activation. Although $V_{OC}$ increased by 30-40 mV in such devices, a significant loss in FF balanced this $V_{OC}$ increment and $J_{SC}$ remained unaffected. We knew that these devices were already recrystallized and might need passivation for higher $V_{OC}$ but the 5-minute activation increases the series resistance of the cells and decrease the FF.

![Figure 3-7. Performance indicators of sputtered CdS/CdTe solar cells.](image)

[Note: red squares = cells received heat treatment without CdCl$_2$ at given temperatures, blue dots = devices received heat treatment (without CdCl$_2$) at given temperatures with an additional 5 minute CdCl$_2$ treatment at 400 °C.]
3.6 **Cell Performance at Higher Temperature CdCl$_2$ Activation**

High efficiency CdTe devices usually receive chloride activation at 390-420 °C for 10-30 minutes. But here we are interested to see the effects of higher temperature activation such that CdTe devices will be seriously overtreated. For this, we prepared a few samples which received a 20-minute CdCl$_2$ activation at 400 °C, 425 °C and 450 °C and were completed with our regular back contact processing. As shown in Figure 3-8(a), the CdTe devices activated at higher temperature exhibited poor cell performance especially in $V_{OC}$ and FF as well as poorer yield due to delamination. The overtreatment causes a $V_{OC}$ loss due to the introduction of S-related defect states [75] and the fill factor loss due to high series resistance.

The quantum efficiency shown in Figure 3-8(b) presents a significant drop of CdS thickness at 400-530 nm when the activation temperature increases from 400 °C to 450 °C due to stronger S diffusion into the CdTe region. At 450 °C, the QE at 450 nm shows no evidence of any residual of the original 80 nm of CdS left over after 20 minutes of activation. The treatment condition was more than enough to drive all CdS into CdTe layer and distributes uniformly so that QE remains unaltered over 450-800 nm. Although CdS absorption changes remarkably with treatment temperature and increases the collection at 400-530 nm, no further improvement in $J_{SC}$ is achieved mainly due to a corresponding decrease in collection at 530-800 nm.

High angle x-ray diffraction data of chloride-treated samples are shown in Figure 3-8(c). With a narrow angle scan from 75-80 degree, stronger diffusion of S into the CdTe was observed as the chloride activation temperature increased from 400 °C to 450 °C. Again using the Vegard relation, the sulfur content in CdS$_x$Te$_{1-x}$ is estimated at
approximately 0.02, 0.05 and 0.07, respectively, for 20 minutes of chloride treatment at
400 °C, 425 °C and 450 °C. This indicates a close agreement with the miscibility data as
observed by McCandless et al. [83], where $x = 0.0685$ for 450 °C. These observations are
consistent with the QE data shown in Figure 3-8(b).
3.7 Sputtered CdS/CdTe Cells Activated With and Without Oxygen

This section explores the effect of oxygen during fabrication process of sputtered CdTe cells. For this, we sputtered the CdS/CdTe films in an oxygen-free ambient and processed with standard CdCl$_2$ activation in N$_2$, Ar or dry air atmospheres. These devices then received standard Cu/Au contacts and finally were annealed for 45 minutes at 150 °C in room ambient. The J-V measurements were performed under solar simulator and the results are shown in Table 3.3.

Compared to dry air ambient, CdTe cells activated in N$_2$ and Ar showed lower $V_{OC}$ by ~50 mV and $J_{SC}$ by ~2 mA/cm$^2$, confirming the advantages of oxygen incorporation in the CdTe film and grain boundary. On the other hand, the fill factor of the cells treated in Ar ambient was improved by 3-4% in absolute measurement but it was
not enough to overcome the drop in $V_{OC}$ and $J_{SC}$ and thus resulted lower efficiency than the cells treated in air. Since our standard fabrication method does not include any chemical etching step, a lower series resistance is anticipated when cells are treated without oxygen and possibly results higher fill factor. When CdTe devices received CdCl$_2$ activation in air ambient, the formation of oxides or sulfates (i.e. TeO$_2$, CdO, CdSO$_4$) likely occurred [84]. The deposition of Cu/Au contacts without removing such compounds could yield lower fill factor.

**Table 3.3: CdTe cell performance vs. CdCl$_2$ treatment ambient.**

<table>
<thead>
<tr>
<th>CdCl$_2$ activation ambient</th>
<th>$V_{OC}$ (mV)</th>
<th>$J_{SC}$ (mA/cm$^2$)</th>
<th>FF (%)</th>
<th>Eff (%)</th>
<th>$R_S$ ($\Omega$-cm$^2$)</th>
<th>$R_{SH}$ (K$\Omega$-cm$^2$)</th>
</tr>
</thead>
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<tr>
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<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Best</td>
<td>839</td>
<td>22.5</td>
<td>71.2</td>
<td>13.4</td>
<td>5.3</td>
<td>2.3</td>
</tr>
<tr>
<td>Average</td>
<td>820</td>
<td>22.5</td>
<td>68.5</td>
<td>12.7</td>
<td>5.7</td>
<td>2.2</td>
</tr>
<tr>
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<td></td>
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<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Best</td>
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<td>19.5</td>
<td>74.0</td>
<td>11.5</td>
<td>3.6</td>
<td>2.1</td>
</tr>
<tr>
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<td>72.2</td>
<td>11.0</td>
<td>4.3</td>
<td>1.9</td>
</tr>
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</tr>
<tr>
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<td>19.7</td>
<td>71.0</td>
<td>11.2</td>
<td>5.0</td>
<td>1.3</td>
</tr>
<tr>
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<td>19.6</td>
<td>68.7</td>
<td>10.6</td>
<td>5.6</td>
<td>1.3</td>
</tr>
</tbody>
</table>

**3.8 Conclusion**

We have studied the effects of post-deposition heat treatments without CdCl$_2$ on sputtered CdS/CdTe thin-film solar cells. Substantial re-crystallization appears to begin near 425 °C but 450 °C was required to reach good electrical performance of cells annealed without CdCl$_2$. CdTe grain size increased from about a hundred nanometers to more than a micron as the polycrystalline texture decreased from the preferred (111) direction of the as-sputtered condition. After 20 minutes annealing at 450 °C the SEM micrographs showed up to 2 µm grains for film thickness of ~2 µm with somewhat different morphology from those CdCl$_2$ activated at 387 °C. When CdTe films received a
heat treatment at 450 °C in dry air without CdCl₂, 11.6% conversion efficiency was observed as compared to ~13% for typical cells activated at 387 °C with CdCl₂. The lower performance reached in the absence of CdCl₂ probably results from poorer grain boundary passivation and perhaps poorer doping of the CdTe film. A short CdCl₂ activation after the 400 and 425 °C heat treatments further improved the \( V_{OC} \) and FF of the CdTe cells.

Sputtered CdTe films receiving CdCl₂ activation at 425 °C and 450 °C showed evidence of stronger sulfur diffusion into CdTe. This situation is often called “overtreated”. With substantial amount of S in CdTe, the density of defect states increases significantly, and these states may act as recombination centers to reduce \( V_{OC} \) and FF. But the \( J_{SC} \) of these devices was not affected due to a decrease in CdS absorption. In addition, the CdTe cells processed without oxygen during CdCl₂ activation exhibited poor \( V_{OC} \) and \( J_{SC} \), indicating the requirement of oxygen during activation.
Chapter 4

Influence of CdS Thickness and Substrate Type on the Stability of Sputtered CdS/CdTe Solar Cells

4.1 Introduction

In the previous two chapters, we introduced some new concepts that are helpful to improve the efficiency of sputtered CdS/CdTe cells. But as the title says, the main goal of this dissertation is to find out the root causes of the instability of sputtered CdTe cells. Although numerous studies on the cell stability have been reported for CdTe cells and modules [45-55], a systematic study on the stability of sputter-deposited CdS/CdTe cells has not been reported. Here, we are interested in all cell parameters and will diagnose them individually to improve the life time of sputtered CdTe cells.

Accelerated life testing (ALT) is the most common way of stressing thin-film solar cells at the laboratory scale [45-50]. ALT can be correlated with field stress conditions; however, solar modules in the field encounter variable temperatures and different biasing conditions. The stability of active layers and their processing parameters play a significant role in device stability and determine the degradation rate. For example, high efficiency CdTe cells can be obtained with a Cd$_2$SnO$_4$/Zn$_2$SnO$_4$ bilayer TCO [18],
but their long-term stability is questionable. Albin et al. [46] reported that CdTe cells prepared on SnO$_2$:F/SnO$_2$ substrate ended up with higher final efficiency than the cells prepared on Cd$_2$SnO$_4$/Zn$_2$SnO$_4$ coated glass substrate after 115 hrs of light soaking test at open-circuit and 100 °C.

In this chapter, we study light soaking effects on sputtered CdS/CdTe cells and correlate degradation rates with substrate type and CdS thickness. The cell performance after 300 hrs of light soaking at 65 °C and open-circuit biasing condition will be discussed.

4.2 Experimental

CdTe cells were sputter-deposited on TEC15 and highly resistive transparent (HRT) layer coated TEC15 glass substrates provided by Pilkington. Thin films were grown on these two types of substrates 3.0” × 1.5” mounted side-by-side at a substrate temperature of 250 °C in the classic system. Seven CdS layer thicknesses were chosen 0, 30, 45, 80, 130, 160 and 230 nm for standard (2.2-2.5 μm) CdTe layers. Following the deposition, all samples received a standard chloride activation and back-contact process, as described in Section 2.2. Prior to chloride activation, as-grown CdTe samples were stored in plastic cases for a few months.

The complete cell structures of each CdS thickness set were divided into two, with one of them light-soaked and the other one stored in the dark in room air. These we call sister cells and used them as a control in this study. The first set of samples was light soaked in a Sun-Test XLS+ system, Figure 4-1, under one sun illumination at 65 °C and $V_{OC}$ biasing condition for a total 300 hours. The current-voltage measurements of the
stressed samples were carried out under AM1.5 illumination after light-soak durations of 1, 3, 10, 30, 100, and 300 hours. To observe faster degradation effects in a short period, cells were not encapsulated and the typical average humidity was recorded as ~40% at room temperature. About ten dot cells of area 0.062 cm² for each CdS thickness were used in this study.

In order to test their recovery behavior, light-soaked sputtered CdTe cells were stored in plastic cases in the room ambient for 65 days.

![Sun-Test XLS+ system](image)

**Figure 4-1.** Sun-Test XLS+ system for light soaking study manufactured by ATLAS. The system uses xenon lamp for illumination. It has capability of temperature control and solar irradiance. The room air flows into the system to maintain the temperature inside the chamber.

### 4.3 Effect of CdS Thickness and Substrate Type on Initial Measurements (t = 0 hrs)

In this section, we discuss the role of HRT layers and CdS thickness on initial performance of sputtered cells. The performance indicators of these CdTe cells are
Figure 4-2. Average performance of seven different thickness CdS cells on TEC15 and HRT-coated TEC15 substrates before light soaking (i.e. $t = 0$ hrs) a) open-circuit voltage, b) fill factor and c) efficiency.

presented in Figure 4-2. It is clear that the HRT layer on top of the TCO enhances the initial performance of the solar cell when very thin CdS is used in the device structure. Without HRT, the solar cells show lower initial performance. $V_{OC}$ and FF are particularly impacted as shown by the data of Figure 4-2(a), and 4-2(b). Both parameters decrease with CdS thickness and the decrease in $V_{OC}$ becomes significant if CdS thickness is less than 130 nm when no HRT is used. This yields wider variation in cell efficiency for thinner CdS cells as reflected by the large error bars, Figure 4-2(c). Generally, the thinner CdS cells show higher short-circuit current (see Figure 2-6). On TEC15 (without HRT) the 10-cell average initial open-circuit voltage ($V_{OC}$) increases from 460 to 800 mV as
CdS thickness increases from 30 nm to 230 nm. The average initial efficiency on TEC15 increases from 6.2 to 10% over the same range of CdS thicknesses, Figure 4-2(c). By contrast on TEC15 with HRT-coatings these initial (t = 0 hrs) open-circuit voltage and efficiency are almost independent of CdS thickness (above 30 nm). In these devices the FF and \( V_{OC} \) deficit is much lower than TEC15 substrates and can be balanced by an enhancement of \( J_{SC} \) due to thinner CdS.

One additional observation is that cells without CdS fabricated on HRT-coated glass generate an average efficiency of 4.5%, while similar CdS-free cells on TEC15 only reach 2%. The average \( V_{OC} \) of these CdS-free cells on HRT-coated glass is 516 mV compared with a \( V_{OC} \) of 270 mV on TEC15. Clearly the interface that forms between the HRT and CdTe is better than that between SnO\(_2\):F and the CdTe.

4.4 Stability Under ALT vs. Substrate (t = 300 hrs)

After light soaking for 300 hours in room air, we found that the relative loss in efficiency is comparable on both substrates (Figure 4-3(a)). However, the CdTe cells on HRT-coated substrates still ended up with higher efficiency than cells on bare TEC15 substrates. As shown in Figure 4-3(b), the representative J-V data show that the degradation mechanisms that occur with the two different substrates might be different. Unlike the cells on HRT-coated glass, CdTe cells on bare TEC15 which exhibited very small loss on \( J_{SC} \), \( V_{OC} \) and FF. Only the FF was observed to be a degradation parameter for the HRT-coated sample. Comparatively strong roll-over effects were observed on the HRT-coated samples indicating either a reverse-diode behavior or significantly large series resistance.
Figure 4-3. a) Average efficiency for seven different CdS thickness cells on TEC15 and HRT-coated TEC15 substrates after light soaking (i.e. $t = 300$ hrs) and b) current-voltage characteristics of two representative cells prepared on bare TEC15 and TEC15 with HRT-coatings substrates. In Figure 4-3(b), both CdTe cells were finished with 230 nm CdS and 2.4 μm CdTe.
4.5 Stability Under ALT vs. CdS Thickness

This section describes the effects of CdS thickness on cells stability while using HRT-coated and bare TEC15 substrates. As shown in Figure 4-4(a), the ten-cell average efficiencies of cells on the HRT-coated substrates distribute in a narrow range between 9.8 and 11% before light soaking for CdS thickness between 30 and 230 nm. This performance decreased to about 6-9% under the given light soaking conditions in room air. The evidence of light soaking effects begins at 10-30 hrs independent of CdS thickness. Among these cells, thicker CdS (> 80 nm) cells are somewhat more stable than thinner CdS cells.

Similar conclusion can be drawn from the cells prepared on TEC15 substrate which exhibited stability behavior very similar to HRT-coated substrate; however, the wide distribution in efficiency due to CdS thickness variation is observed in these cells, Figure 4-4(b). But it should be noted that the efficiency of CdTe cells on the HRT-coated substrate ended up with higher efficiency when thinner CdS is used, Figure 4-3(a). In most cases, a first-quadrant roll-over effect is observable between 30-300 hrs as shown in the J-V measurements of Figure 4-5(a) and 4-5(b). Comparing J-V measurements of the 30 nm with the 230 nm CdS cells, we observe that the thicker CdS cell loses mostly FF during 300 hrs of light stressing in air while thinner CdS cells lose FF, V<sub>OC</sub> and J<sub>SC</sub>.

It should be noted that the testing procedure used here involved removing the cells from the light soak chamber and individually contacting the cells for testing under the solar simulator at room temperature. Contact was made with a spring-loaded “pogo” pin. In a few cases, this process resulted in some visible damage to small areas of the
Figure 4-4. Average efficiency for seven different CdS thickness cells during 300 hrs of light soaking at 65 °C, open-circuit voltage biasing and no encapsulation; a) on HRT-coated TEC15 substrate and b) bare TEC15 substrate.
**Figure 4-5.** Typical J-V characteristics of the best CdTe cells on HRT-coated TEC15 substrate for two different CdS thicknesses; a) 30 nm b) 230 nm.

cells. If probe damage was visible to the naked eye, we removed the cells from the study set. In addition, there might be probe damage not visible to the eye which would produce a small area of reduced response, we cannot rule out this as a contributing factor to
reduced performance on these small area cells which have thin metal back contacts (3 nm Cu + 20 nm Au).

To determine more information about the degradation mechanism, the cell performance parameters were plotted in a manner that permitted correlations could be observed. Figure 4-6 shows a statistical correlation between the change in efficiency vs. change in $V_{OC}$, FF and $J_{SC}$ for 10 CdTe devices for each CdS thickness used in this study. The data show a strong correlation between the change in efficiency and the change in FF for all CdS thicknesses. But the correlation between efficiency and $V_{OC}$ or $J_{SC}$ varied according to the CdS thickness.

For example, the decrease in efficiency of the 30 nm CdS cell strongly depends on $V_{OC}$, FF and $J_{SC}$ whereas the efficiency for cells with 230 nm CdS depends primarily on FF. Because of interdiffusion during chloride activation [30], the final CdS thickness of 30 nm CdS devices would be reduced to <10 nm. In such devices, the continuous illumination easily depletes the n-type layer and reduces the electric field at the junction. This effect essentially causes poorer collection away from the junction and thus produces lower $J_{SC}$. But with thicker CdS, this effect would be minimal.

Figure 4-7 presents the relative measurement of the cell performances after 300 hrs of ALT for cell with different CdS thickness compared with similar stored samples. It shows that the stability of sputtered cells is independent with the substrate type. Although there is no clear trend of stability as a function of CdS thickness, thicker CdS cells are weakly affected in comparison with thinner CdS cells. For some CdS thicknesses (i.e. 45 nm and 130 nm) it can be observed that some CdTe cells lost only 3-
Figure 4-6. Statistical correlation between the change in efficiency vs. change in $V_{OC}$, FF and $J_{SC}$ of CdTe cells for two CdS thicknesses; a) 30 nm and b) 230 nm.
5% efficiency in relative measurement. This indicates the possibility of further improvement after careful optimization in fabrication parameters. More details of this study will be discussed in Chapter 6. Like light-soaked cells, the relative efficiency of sister cells follows a similar stability trend with CdS thickness.

**Figure 4-7.** Relative measurements of the cell efficiency of CdTe cells for t = 300 hrs and t = 0 hrs as a function of CdS thickness. The devices were prepared on HRT-coated TEC15 and bare TEC15 substrates.

Sputtered CdTe cells stored for 65 days at room temperature in room ambient after 300 hrs of light soaking (ALT) recovered some performance, Figure 4-8. Solar cells with < 80 nm CdS did not exhibit any recovery on either substrate. Unlike thinner CdS, the average efficiency of thicker cells either improved or remained the same. Cells without CdS deteriorated further on both substrates. This might be related to the TCO/CdTe junction formation which may not be as stable as the CdS/CdTe junction. So it can be proposed that a thick enough (> 80 nm) CdS layer is essentially required to produce the decent stability of CdTe cells.
Figure 4-8. Ratio of the cell efficiency of CdTe cells after two months dark storage to $t = 300$ hrs light soaking. For recovery test, the devices were stored in drawer for two months in room light ambient.

4.6 Conclusion

We have performed a light soaking study of sputtered thin-film CdS/CdTe solar cells with seven different CdS thicknesses and two different substrates. The devices were stressed under one-sun illumination, at 65 °C, open-circuit biasing and no encapsulation in room ambient over 300 hrs. About 40% average relative humidity at 25 °C was measured during soaking period. From this study, we find that cells with > 80 nm CdS have somewhat better stability. On these cells, the HRT layers help to produce high initial performance and better uniformity by maintaining high $V_{oc}$ as well as FF for thin CdS layers. After 300 hrs, cells which have more than 80 nm of CdS end with quite similar performance, independent of the presence of this HRT layer. We conclude there is no direct evidence to indicate that this HRT layer improves the stability of sputtered cells.
under one-sun light soak at open-circuit and no encapsulation, but it is very effective in yielding improved initial efficiency with very thin CdS layers.
Chapter 5

Influence of CdTe Thickness on the Stability of Sputtered CdS/CdTe Solar Cells

5.1 Introduction

In Chapter 4, the study of the long term stability of sputtered CdTe cells was mainly focused on substrate types and CdS thicknesses where we used two different substrates (with and without highly resistive layer coated TEC15 glass) and seven different CdS thicknesses from 0 nm to 230 nm. Here we are interested to study the effects of CdTe thickness on cell stability.

It is well known that reducing the thickness of CdTe films is advantageous for material usage to reduce Te consumption in CdTe solar modules and increase deposition speed thus decreasing the production cost. Unfortunately, thinning the CdTe below 1 μm is challenging because it increases shunting effects and reduces photons absorption [64, 65]. However, we successfully fabricated thinner CdTe cells on SnO₂:F glass substrates which have reached 12.5% efficiency for 0.75 μm absorber layer thickness (see Table 2.3). This is the highest efficiency ever reported for that thickness and is very encouraging for ultrathin device fabrication because the efficiency is comparable with the
efficiency of commercial CdTe module [12]. Therefore, we are motivated for further study on long term stability of such devices. Stability is critically important to demonstrate before manufacturing.

In this chapter, we compare the stability results of sputtered CdTe cells of thickness 0.7-2.1 μm after 900 hrs light soaking test at 85 °C, V_OC biasing and no encapsulation. The cell performance results will be discussed after current-voltage and quantum efficiency measurements. The feature analysis of the thin-film samples are further explained with secondary ion mass spectroscopy (SIMS) depth profiles of various elements such as Cu, Cl, S, O.

5.2 Experimental

Polycrystalline CdTe films of thicknesses 0.7, 1.1, 1.6 and 2.1 μm were prepared on Pilkington HRT-coated TEC15 glass substrate after 100-110 nm of sputtered CdS. Following the deposition, the devices received CdCl₂ activation at 387 °C. As suggested in Chapter 2, shorter activation times were favorable for cells having thinner CdTe which we estimated here by using Equation 2.1 and Arrhenius behavior. An optimum Cu/Au contact was applied to the CdTe samples as suggested by the fit in Figure 2-9. The device fabrication parameters we used in this study are given in Table 5.1.

In order to observe stronger effects we increased the temperature and duration of the stressing period. The light soaking test was continued in the Suntest XLS+ system with unencapsulated CdTe cells which were illuminated under one sun at 85±3 °C, V_OC biasing and room ambient for 900 hrs. More than 20 dot cells of area 0.12 cm² for each CdTe thickness were prepared for this study. We reduced the number of J-V
measurements to avoid possible *pogo stick* damage that occurred in the previous stability study (Chapter 4). With identical processing parameters, we prepared a second set of devices used as control which were stored in desiccated air under room light illumination. Light-soaked CdTe cells were further “rested” in room light ambient for 32 days for a test of whether any performance recovery would occur.

**Table 5.1:** Post-deposition parameters for various thickness CdTe cells. The fabrication parameters were chosen according to Arrhenius behavior and the straight line fitting shown in Figure 2-7 and 2-9. The CdCl$_2$ activation temperature and copper diffusion temperature were respectively set at 387 °C and 150 °C.

<table>
<thead>
<tr>
<th>CdS/CdTe thickness (μm)</th>
<th>CdCl$_2$ treatment time (min.)</th>
<th>Cu/Au thickness (nm)</th>
<th>Cu diffusion time (min.)</th>
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<td>0.11/2.1</td>
<td>35</td>
<td>3.0/20</td>
<td>45</td>
</tr>
</tbody>
</table>

**5.3 Effect of CdTe Thickness on Initial Measurement (t = 0 hrs)**

About 11.0 - 13.0% efficiency was achieved on the sputtered CdTe cells for 0.7 - 2.1 μm CdTe on HRT-coated TEC15 glass substrates, Figure 5-1. As expected, we observed lower efficiency on thinner cells, primarily due to incomplete photon absorption. In addition, poorer FF and $V_{OC}$ was also observed for 0.7μm CdTe cells with much larger cell to cell variation must be related to shunting. As observed in Figure 5-1(b), the conversion efficiency of CdTe cells decreases with absorber layer thickness and falls quickly below 1μm (see Figure 2-11) is mainly due to poorer absorption.
The quantum efficiency (QE) measurement of four different CdTe cells is shown in Figure 5-2. As expected, thinner cells have deep penetration loss due to insufficient...
absorption of red photons clearly observed on the slope differences at 700-800 nm. The absorption loss due to CdS-CdTe interdiffusion (at 500-600 nm) is quite similar for all thickness indicating nearly optimum chloride activation condition for thinner cells as well even though they treated for shorter period.

![Graph showing external quantum efficiency](image)

**Figure 5-2.** External quantum efficiencies of four different CdTe cells.

### 5.4 Stability Under ALT vs. CdTe Thickness (t = 900 hrs)

#### 5.4.1 Current-voltage (J-V) Measurements

In this section, we compare the results of cell performance after performing accelerated life testing (ALT). Comparing with the results from Chapter 4, we observed better stability of sputtered CdTe cells despite the fact that they were tested at higher temperature (85 °C) and for longer period (900 hrs). Remember that the CdS series was studied at 65 °C for 300 hrs. Devices show no clear trend of thickness dependent
stability. But standard CdTe cells (2.1 μm) which started with higher efficiency were also ended with higher efficiency, Figure 5-3. Any CdTe cells which showed degradation exhibited a drop in $V_{OC}$. Such $V_{OC}$ dominated effects had not been observed in Chapter 4. This might be correlated with the testing temperature as suggested by Albin et al. [46].

**Figure 5-3.** Normalized cell performance parameters of solar cells made with four different CdTe thicknesses; a) open-circuit voltage, b) short-circuit current c) fill factor and d) efficiency. An average of 20 dot cells was plotted as a function of stressing hours on a logarithmic scale. CdTe cells were light soaked for 900 hrs at 85 °C, $V_{OC}$ biasing and room ambient.
Under given ALT conditions, about 60-100 mV of $V_{OC}$ was lost for the CdTe cells that were less than 2 μm thick but the decrease was ~ 20 mV for the standard CdTe thickness (Figure 5-3(a)). Contrary to change in $V_{OC}$, less than 1 mA/cm$^2$ was lost in $J_{SC}$ (Figure 5-3(b)), and only a 1-3 % drop in FF (Figure 5-3(c)) was observed. We suspect that the change in short-circuit current density might be due to experimental uncertainty rather than a true loss. With these changes, about 7-15% relative loss in efficiency was observed for more than 80 devices (Figure 5-3(d)). We believe these results are very promising for sputtered CdTe cells. Further stability improvements can be made with careful optimization of post-deposition parameters and through encapsulation.

The results described above can be examined in terms the statistical correlation between cell performance parameters. Figure 5-4 shows the correlation between the change in efficiency and change in $V_{OC}$, FF and $J_{SC}$ for more than 80 CdTe cells used in this study. The data show a strong linear correlation between change in efficiency and change in $V_{OC}$ for all CdTe thicknesses suggesting $V_{OC}$ dominated loss. In Figure 5-4(a), most cells with standard thickness show less than 5% changes in $V_{OC}$, which produced 3-6% loss in the efficiency. But most of the cells that are dispersed in 7-17% range of $\Delta V_{OC}$ are from thinner cells which yielded 7-22% change in efficiency. On the other hand, the correlation between $\Delta \eta$ and $\Delta J_{SC}$ (Figure 5-4(b)) or $\Delta \eta$ and $\Delta FF$ (Figure 5-4(c)) is much lower than the correlation between $\Delta \eta$ and $\Delta V_{OC}$ (Figure 5-4(a)). We observed less than 5% effect on these cell parameters. As shown in Figure 5-4(c), some devices showed negative changes in $\Delta FF$ indicating improvement in FF after ALT, surprisingly these cells were from standard CdTe thickness. But a loss in $V_{OC}$ balances the FF improvement leading to minimal overall light soaking effects.
Figure 5-4. Statistical correlation between the cell performance parameters after 900 hrs light soaking test. The change in efficiency is plotted as a function of; (a) change in $V_{OC}$, (b) change in $J_{SC}$ and (c) change in FF. Furthermore, we analyzed series and shunt resistances of light-soaked cells to understand the typical loss in $V_{OC}$ and FF. Two graphs shown in Figure 5-5 (a) and 5-5(b) are box and whisker plots of resistances measured at $t = 0$ hrs (before light soaking) and at $t = 900$ hrs (after light soaking). Light-soaked samples showed same directional changes of both resistances except in the case of 0.7 μm CdTe cells. An improvement of shunt resistance of these devices increase the fill factor but at the same time the series
Figure 5-5. Box and whisker plot of: a) series and b) shunt resistance of various CdTe solar cells light soaked without encapsulation under one-sun illumination at 85 °C, $V_{OC}$ biasing condition in the room ambient. The upper and lower limits of box and whisker plots are 75-25% and 95-5% respectively; middle line of box – median; small dot inside the box – mean.

... resistance also increased. Since we observed greater effect of series resistance, the overall FF was decreased by 5% in relative measurement. In the case of the 0.7 μm CdTe cells,
the decreased shunt resistance might be attributed to further diffusion of Cu and resulted lower FF. Among four different thicknesses, 1.6 μm CdTe cells were the most affected in ALT series, exhibiting noticeable jumps in their series resistances.

5.4.2 Secondary Ion Mass Spectroscopy (SIMS)

SIMS depth profiles of the sputtered samples were taken at NREL. For this measurement, we sent standard CdTe samples to NREL after various growth steps (i.e. as grown, CdCl₂ activated, complete device structure and 300 hrs light-soaked CdTe cells). The depth profiles were obtained on a Cameca IMS-5F using an O₂⁺ primary ion beam at 12.5 kV for detection of positive secondary ions and a Cs⁺ source at -202 V for detection of negative ions. The mass spectrometer was tuned for mass resolution m/Δm ~ 4000.

Figure 5-6 shows the Cu profile into CdS/CdTe cells which is quantified here, has higher concentration in CdS region than CdTe. The Cu level increases up to 2x10¹⁷ cm⁻³ and distributes uniformly inside the entire CdTe region after device gets CdCl₂ activation confirming the residual Cu from CdCl₂ powder. After contacting with Cu, the concentration jumps to 10²¹ near CdTe/Cu interface, and more Cu ions diffuse into CdTe. Clearly two types of Cu diffusion profile (0-1 μm and 1-2 μm) can be observed into CdTe film. In the first 1 μm depth, sputtered CdTe film has shown relatively more porous structures and grain boundaries such that more Cu allows to diffuse through and gets higher concentration but beyond that point (1 - 2 μm region) the void fractions decreases to ~ 2% with fewer grain boundaries [85] so that slow diffusion is expected. For ALT cells, the SIMS profile of Cu is unchanged within experimental error, including negligible changes in the CdS layer.
Figure 5-6. Concentration profile of Cu in sputtered CdS/CdTe cell after different processing steps. The SIMS depth profile was taken from the back contact side of the device and calibrated with Te counts.

The diffusion of Cu into CdTe occurs through three different mechanisms; interstitial (Cu\textsubscript{i}), substitutional (Cu\textsubscript{Cd}) and grain boundary diffusion. Interstitial Cu\textsuperscript{+} ions, which are actually shallow donors (0.01 eV), are highly mobile; substitutional Cu\textsubscript{Cd} states are shallow acceptors (0.2 eV) and less mobile [14]. In the case of UT’s standard deposition method, the heat treatment at 150 °C after Cu/Au evaporation is the final step of CdTe cell fabrication that introduces Cu into CdTe. If the primary diffusion mode of copper is through interstitial Cu\textsuperscript{+} [51, 57], then the electric field across the junction will play an important role depending on the cell bias conditions. In the dark, when Cu\textsuperscript{+} ions reach the depletion region, the electric field prevents the further diffusion. This phenomenon can explain the difference in Cu gradients in Figure 5-6 when the depletion region of CdTe side is extended nearly 1 μm away from the CdS/CdTe interface.
The diffusion of Cu into CdTe under continuous illumination at elevated temperature and different biasing condition can be explained as suggested by Hegedus, et al. [50] and Hiltner and Sites [57]. If accelerated life testing (ALT) is performed under short-circuit biasing, (the band diagram shown in Figure 5-7(a)), an electric field across the junction remains and will tend to inhibit further diffusion of Cu$^+$ ions so that CdTe devices show better stability. At open-circuit condition, the photo-voltage developed across the two contacts of the device structure will keep the CdTe cell at forward bias (with open-circuit voltage) and reduces the depletion region as well as the electric field (Figure 5-7(b) shows the case of zero electric field). Under this condition, the diffusion of Cu$^+$ ions is not inhibited by a field and the cell is expected to degrade more severely than at short-circuit or maximum power-point condition. In our case, Figure 5-6 shows little diffusion of Cu during ALT showing that sputtered cells are promisingly stable at open-circuit biasing, provided back contact process is optimized carefully.

![Figure 5-7](image)

**Figure 5-7.** Sketch of band diagram of SnO$_2$:F/CdS/CdTe/metal structure under one sun illumination at different biasing conditions; a) short-circuit biasing and b) open-circuit biasing.

It is also important to understand the effects of Cl, S and O on the cell stability. Therefore, we also analyzed the SIMS depth profiles of such elements to trace their
distribution before and after stressing. The secondary ion counts of these species present in sputtered CdTe cells are plotted in Figure 5-7. For low-temperature processing, the diffusion of sulfur occurs in CdCl$_2$ activation process (Figure 5-8(a)) which drives significant increase (more than two orders of magnitude) of S on the back contact side of the CdTe layer. Sometimes the sulfur may have chance to combine with Cd and O to form CdSO$_4$ which is harmful for CdTe device [84]. After 300 hours light soaking, the S signal is unchanged within experimental uncertainty.

Similarly, a very uniform distribution of Cl in CdTe can be seen after the chloride activation; however, some level of Cl was already present in as-grown films (Figure 5-8(b)). After light soaking, we did not observe any evidence of Cl migration in CdTe. Furthermore, a clear indication of O incorporation into CdTe film from the contact side is observed after CdCl$_2$ activation which was done in dry air ambient, Figure 5-8(c). As detected in as-grown sample, 270 °C substrate temperature is more than enough to diffuse O from TCO layers to CdS/CdTe region.
Figure 5-8. Secondary ion counts of various elements in sputtered CdS/CdTe solar cells; a) sulfur b) chlorine and c) oxygen. The secondary ion counts are calibrated with calibrated with Te counts.
With these observations, the instability appeared on the sputtered CdTe cells is not associated with the migration of Cu, S, Cl and O when the light soaking conditions are set at 85 °C and Voc biasing.

5.5 Light-soaked Cell Performance After Dark Rest

In this section we discuss the possible recovery of sputtered CdTe cells after samples have received ALT. The CdTe cells were tested after 32 days of rest in room light ambient. In this series, cells with 1.1 μm and 1.6 μm CdTe layers were much more greatly affected by lost > 60 mV V_{oc}. Such devices have shown up to 30 mV recovery in V_{oc} without affecting their J_{sc} and FF. But the cells affected weakly in ALT neither recovered nor further degraded, Figure 5-9. Thus, the larger the degradation results, the better the recovery for sputtered CdTe cells. On the other hand, the sister cells which were rested for 75 days in desiccant ambient were unaffected within ± 2% error of current-voltage measurement.

5.6 Lifetime Projection of Sputtered CdS/CdTe Solar Cells

Hiltner and Sites [57] have proposed that a temperature dependent degradation mechanism of some CdS/CdTe solar cells is characterized by a 1 eV activation energy. For E_{a} = 1 eV, the estimated acceleration factor is 1000 when devices receive light soaking at 100 °C and V_{oc} biasing in room ambient. Assuming that our sputtered cells are also characterized by E_{a} = 1 eV, we also estimated the field lifetime of our sputtered CdS/CdTe cells using Arrhenius relationship [60]:

\[ R_T = \exp \left( -\frac{E_a}{K_B T} \right) \]
Figure 5-9. Relative efficiency as a function of absorber layer thickness for CdTe solar cells that received either ALT conditions or room light ambient storage. Data points with black solid squares are for light soaked cells measured with respect to initial efficiency where red dots are after recovery test measured with respect to light-soaked efficiency. [Note: Cells labeled with blue cross symbols are sister cells measured after 75 days in desiccant ambient rest with respect to initial efficiency.]

Where \( R_t \) is rate of degradation, \( E_a \) is the activation energy, and \( K_B \) is the Boltzmann constant. When sputtered cells receive light soaking at 85 °C and \( V_{OC} \) biasing, the acceleration factor becomes 270. After using average daily sun hours i.e. 5.5 hrs/day, which is an average for the major cities of United States for a year [86], we estimated roughly 120 years lifetime of sputtered CdS/CdTe cells in the field with less than 15% loss in efficiency. That suggests an average drop of 0.1% per year.

5.7 Conclusion

Under given ALT, an average drop of 7-15% in relative efficiency was observed on sputtered CdTe cells after 900 hrs of light soaking at 85 °C in room air at \( V_{OC} \).
Comparing with thinner devices, standard CdTe cells show better stability. The degradation of all sputtered cells was mainly dominated by $V_{OC}$ loss. Very little drop in FF was attributed to the same directional changes (increment) of series and shunt resistances of CdTe cells. After ALT, no indication of further diffusion of Cu had been observed in SIMS profile when 3 nm Cu was used at back contact. It also suggests that the interdiffusion of various elements i.e. S, Cl, O occurs at the high temperature CdCl$_2$ activation step not in ALT. Like close-spaced vapor transport cells [55], sputtered CdS/CdTe cells which lost $V_{OC}$ by $>60$ mV in ALT had shown about 30 mV recovery after 32 days rest in room light ambient. Furthermore, we estimated 120 years field lifetime of sputtered CdS/CdTe cells within 15% loss.
Chapter 6

Influence of CdCl$_2$ Activation and Cu Thickness on the Stability of Sputtered CdS/CdTe Solar Cells

6.1 Introduction

In this chapter, we discuss the effects of post-deposition parameters on cell stability where we use CdCl$_2$ activation time and Cu thickness as two independent variables. This chapter explains the effects of these two parameters on fresh cells (t = 0 hrs) and after accelerated life testing (t = 900 hrs). Sputtered CdTe cells used in this study will get a wide range of treatment time (i.e. 10, 25, 40 and 60 minutes) at 387 °C and Cu thickness (i.e. 0, 1, 3 and 10 nm) at the back contact. The results are explained on the basis of current-voltage (J-V), photoluminescence (PL) and secondary ion mass spectroscopic (SIMS) analysis.

6.2 Experimental

Thin films of CdS/CdTe were again prepared on Pilkington's standard highly resistive layer coated TEC15 glass with sputtered 130-160 nm thick CdS followed by 2.1-2.5 μm thick CdTe. In the stability study, we consistently used HRT-coated substrate which has a slight advantage on cell performance before and after ALT. As-grown
samples were then processed with the standard CdCl$_2$ treatment and back contact processing as described in Section 2.2. The chloride treatment time was varied for 10, 25, 40 and 60 minutes at 387°C in dry air and the Cu thickness was chosen to be 0, 1, 3, and 10 nm for each quarter piece of CdTe sample, shown in Figure 6-1. 14 dot cells were finished for each plate with distinct CdCl$_2$ treatment time and Cu thickness.

Figure 6-1. Top view of sputtered CdS/CdTe cells on HRT-coated TEC15 glass substrate. Dot cells of area 0.062 were prepared for four different Cu thicknesses as labeled in a quarter plate of 3”×3” sample. The white shiny part around two sides of the plate is indium bus line is contacted with TCO for J-V measurement.

The first set was given for the light soaking stress at 85 °C and $V_{OC}$ biasing for 900 hrs in room ambient as described in Section 5.2; the second set of samples were stressed in the dark at 105 ± 5 °C again at $V_{OC}$ biasing for 900 hrs. Periodic J-V measurements were carried out on both sets of samples (i.e. light soak and thermal stress) after the cells had cooled to room temperature (RT). The baseline efficiency of the standard devices used in this study was >11%.
6.3 Effects of CdCl\textsubscript{2} Activation on Initial Measurements (t = 0 hrs)

As we have discussed in Chapter 3, the fresh cell performance of sputtered CdS/CdTe cells is sensitive to the temperature and duration of the CdCl\textsubscript{2} activation process. To achieve high efficiency cells, the sputtered CdS/CdTe devices need optimal chloride activation that enhances grain boundary passivation, re-crystallization as well as the electrical properties of the films. The diffusion of S & Te occurs at the interface and controls alloying to form CdS\textsubscript{x}Te\textsubscript{1-x}. We discovered that x = 0.02 [87] is nearly optimal chloride activation condition for sputtered cells. The open-circuit voltage is one of the performance parameters most sensitive to the CdCl\textsubscript{2} variation. The average $V_{OC}$ increases with chloride activation time at 387 °C up to 40 minutes treatment then starts to drop at 60 minutes of treatment, shown in Figure 6-2. Below 25 minutes the $V_{OC}$ will be

![Figure 6-2](image)

**Figure 6-2.** Open-circuit voltage vs. CdCl\textsubscript{2} treatment time at 387 °C of sputtered CdTe cells processed with two different Cu thicknesses at the back contact. The average voltage of 14 dot cells is plotted for each treatment condition.
less than 800 mV and we describe the cells as “undertreated”. At 60 minutes \( V_{OC} \) is again lower and we describe the cells as “overtreated”. In the first case, the inter-diffusion between CdS and CdTe would be insufficient and resulting poorer electrical properties, leads too much inter-diffusion producing higher defect density related to Cl and S to yield lower \( V_{OC} \).

To understand the defect states, PL spectra of chloride-activated CdS/CdTe films were studied at 10 K with 9 mW argon ion laser of wavelength 514.5 nm. As shown in Figure 6-3, the dominant peak around 1.44 eV arises mainly from donor-acceptor pair (DAP) transitions is related to the defect states; Cd vacancy-Cl donor \( (V_{CdCl_{Te}})A \) centers, [82] which are strongest for the overtreated (60 min) sample. At the bound-exciton region near 1.59 eV (Figure 6-3, inset), the overtreated cell shows a second peak.

**Figure 6-3.** Contact-side PL of treated CdS/CdTe films measured at 10 K after four different CdCl\(_2\) activation times. The devices were excited with 514.5 nm argon ion laser with 9 mW power.
near 1.57 eV which is due to alloying of S with the CdTe [14]. Note that this PL arises from the contact side (i.e. “film-side”) indicating the presence of CdS\textsubscript{x}Te\textsubscript{1-x} alloying at the back contact after long treatment times is also observed in SIMS depth profile, Figure 5-7(a). The presence of some S at the back contact has been confirmed with EDS, and XES spectroscopies even at 2 minute treatment times [51, 84], but the PL indicates greater alloying at 60 minutes.

**6.4 Effects of Cu Thickness on Initial Measurements (t = 0 hrs)**

The short-circuit current and fill factor are two other cell parameters which are sensitive to the Cu thickness at the back contact. Little difference in \(J_{SC}\) is observed (Figure 6-4) between 1 nm and 3 nm (or even 10 nm) of copper at the back contact, but if

![Figure 6-4](image)

**Figure 6-4.** Variation of short-circuit current (left) and fill factor (right) as a function of Cu thickness at back contact of sputtered CdTe cells. The performance was observed for 40 minutes of chloride activation time at 387 °C. The average value of 14 dot cells is plotted for each Cu thickness.
no Cu is used, the $J_{SC}$ drops substantially (20-30%). Likewise, FF is also comparable in cells prepared with 1 nm and 3 nm Cu but decreases if the back contact uses more than 3 nm of Cu or no Cu. However, we are able to fabricate cells without Cu at the back contact with an average efficiency ~10 % (Figure 6-5). CdTe cells completed with 10 minutes of chloride activation and 10 nm Cu showed lower efficiency than the cells with 25 minutes activation and no Cu. This indicates the fact that both parameters are critically sensitive for the cell fabrication process.

![Graph](image)

**Figure 6-5.** Average efficiency of sputtered CdTe cells processed with various activation times at 387 °C and different Cu thickness at the back contact.

In order to trace Cu in CdTe, the depth profile was taken for samples with three different Cu thicknesses (0 nm, 3 nm and 10 nm Cu) by using SIMS. The SIMS data show concentration differences in the CdTe layer, (Figure 6-6). 3 nm and 10 nm of Cu in back contact result in a Cu gradient after diffusion but with no intentional Cu, the SIMS profile shows a nearly uniform distribution of Cu at the low $10^{17}$ cm$^{-3}$ level. In the as-
sputtered film, (Figure 5-6), this Cu level is much lower. Since it is known that Cu is highly mobile in CdTe and the 387 °C activation temperature is sufficient to drive in residual Cu from the CdCl₂. Therefore, a couple of nm of Cu is more than enough to dope CdTe region at the back surface and makes a good ohmic contact for our standard sputtered devices. Though some additional Cu (>3 nm) helps to increase the $J_{SC}$ of the device, the $V_{OC}$ and FF decrease with thicker Cu so that the resulting efficiency does not exceed the optimized value (1-3 nm). For 3 nm and 10 nm thickness, the Cu profile in the first 1 μm depth from the back contact side shows significant difference in concentration but beyond that point (1-2 μm) it varies within marginal error suggesting that the E-field is limiting the diffusion of more Cu⁺ towards the junction side.

**Figure 6-6.** SIMS profile before stressing from a sputtered CdS/CdTe solar cells prepared with 40 minutes of CdCl₂ activation and with 0 nm, 3 nm and 10 nm of Cu.
6.5 Stability Under ALT vs. CdCl₂ Activation (t = 900 hrs)

The normalized efficiency of CdTe cells for four different activation times for light and dark stressing conditions are respectively shown in Figures 6-7(a) and 6-7(b). Stability is not very dependent on CdCl₂ treatment time at 387 °C with 3 nm of Cu under light soak stress but thermal stress at higher temperature (105 °C) yields somewhat greater variability and larger decreases for undertreated or overtreated cells. Among them, 40 minutes treatment exhibits better stability in this series with a decrease of an average of 5% in relative efficiency. The degradation is mainly due to a decrease in \( V_{OC} \) (by 75-100 mV) for over-treated (60 min) cells and a decrease in fill factor of 5-7 % for undertreated (10 min) cells. This suggests the devices finished without proper post-deposition optimization introduce more defect states after ALT which causes more performance degradation.

The performance and stability results are consistent with the fact that considerable grain growth and defect removal occurs in these sputtered cells during chloride activation. Enzenroth et al. [88] suggested that extended treatment may introduce excess Cl in grain boundaries and possibly in grain interiors into the CdTe film leads to deterioration. As we observed in Figure 3-8(b), the longer activation also results excess S diffusion in sputtered CdTe cells and enhances defect states. After stressing, the number of defect states are further increased and results \( V_{OC} \) loss. But short activation results insufficient grain boundary (GB) passivation so that CdTe films show poorer electrical properties. These devices will be further degraded after stress and causes FF loss. In addition, optimally processed solar cells limit the grain boundary diffusion of Cu into the CdTe layer also enhancing long-term stability [89].
Figure 6-7. Normalized average efficiency of 14 dot CdTe cells after 900 hrs of stress processed with different CdCl$_2$ treatment time and 3 nm Cu at the back contact; a) light stress at 85 °C and b) thermal stress in the dark at 105 °C.
6.6 Stability Under ALT vs. Cu Thickness (t = 900 hrs)

Like the chloride activation time, the Cu thickness in sputtered cells also has significant impact on the cell stability. CdTe cells with 1-3 nm Cu and 40 minutes of CdCl$_2$ activation time exhibit better long-term stability (Figure 6-8). The change in efficiency of these devices is mostly driven by a decrease in $V_{OC}$ for devices with no intentional Cu. But for cells with 10 nm of Cu at the back contact, the decrease arises primarily from FF and $J_{SC}$ changes. After 900 hrs of stress, the decrease in FF for 1-3 nm Cu is $< 5\%$ in relative measurement but this loss jumps to 60$\%$ for undertreated cells with 10 nm Cu.

![Figure 6-8](image)

**Figure 6-8.** Normalized average efficiency of 14 dot CdTe cells after 900 hrs of light soaked processed with 40 minutes CdCl$_2$ treatment time at 387 °C and various Cu thicknesses at the back contact.

The degradation mechanism of CdTe cells under thermal stress condition is different than light soaking. Under illumination, the excess diffusion of Cu$^+$ ions is
limited due to repulsive interaction with the holes but in the dark, the diffusion enhances without any restriction. As shown in Figure 6-9, the instability of such devices increases with amount of Cu used in the back contact for all chloride treatment times. Cu diffusion primarily causes the degradation of these cells. In contrast to Cu-contacted cells, Cu-free devices improved their efficiency up to 25% during thermal stress in a wide range (10-60 minutes) of treatment time (Figure 6-9). After 900 hrs thermal stress, these devices actually showed higher FF and $V_{OC}$ indicating an improvement of doping level in the contact side may be due to Au diffusion that partly reduces recombination issues. But a representative J-V measurement shows a “roll-over” effect after few hundred hours thermal stress (no illumination) though overall cell efficiency is increased (Figure 6-10).

**Figure 6-9.** Normalized average efficiency of 14 dot CdTe cells after 900 hrs of thermal stress at 105 °C with different chloride treatment times and different Cu thickness in the back contacts.
Figure 6-10. Typical J-V characteristic of the CdTe cell processed without Cu (only 20 nm Au) at back contact and thermal stressed under given ALT conditions. The device was activated for 25 minutes for CdCl$_2$ treatment.

Figure 6-11. Average efficiency of 14 CdTe dot cells after 900 hrs of light soaking processed with four different CdCl$_2$ treatment times at 387 °C and three different Cu thicknesses at the back contact.
Figure 6-11 summarizes the variation in efficiency of the CdTe cells as a function of chloride treatment time for three different Cu thicknesses after 900 hrs of ALT. CdTe cells treated for 25 and 40 minutes with a 3 nm Cu layer at the back contact were the most stable and ended up with the highest efficiency in the series. Compared with the cell performance measured at $t = 0$ hrs (Figure 6-5), we estimated an average of 5% relative loss in efficiency of these CdTe cells.

The instability that appeared in CdTe cells with thicker Cu at the back contact can be further explained by the SIMS data analysis. SIMS profiles taken on light soaked CdTe cells for two different Cu thicknesses are compared in Figure 6-12. For 3 nm of Cu, the depth profile is unchanged within experimental error after 300 hrs of continuous light soaking. For both the stressed and unstressed cells with 3 nm Cu, the Cu concentration decreases monotonically away from the CdTe/CdS interface. This supports the other results shown here, namely, that the sputtered CdS/CdTe cells with evaporated Cu/Au contacts can be very stable if optimized values are applied for the copper thickness and the chloride activation conditions [59]. However, the stressed cell with 10 nm Cu has an increase in Cu concentration, starting at 1 µm from the back surface, increasing to the CdTe/CdS interface. The resulting increase in Cu at the junction causes significant degradation of the main junction explaining the >60% drop in relative efficiency.
The driving mechanism of the Cu diffusion in CdTe cells due to different Cu thicknesses can be understood using the model provided by Corwine et al. 2004 [52]. As shown in Figure 6-13, for thinner Cu at back contact, further bending of CdTe band occurs so that limited Cu$^+$ ions are expected to diffuse into CdTe. But when an excessive amount is present at the contact side, the CdTe band flattens and easily allows more Cu$^+$ ions diffusion towards the junction. As described in Section 5.4.2, at thermal equilibrium, the built-in field inhibits Cu$^+$ diffusion. When CdTe cells are subjected to light soaking at elevated temperature, continuous diffusion results an accumulation of Cu$^+$ ions near the edge of depletion region. Under $V_{OC}$ biasing, the depletion region and E fields are reduced, as shown in Figure 5-7(b), and cannot further limit the Cu diffusion. Thus excessive Cu$^+$ ions are allowed to diffuse towards the CdS/CdTe interface. This could be a plausible explanation of the Cu gradient which was changed in 10 nm Cu after ALT.
At thermal equilibrium, built-in $E$-field will inhibit $Cu^+$ diffusion toward the junction. At $V_{OC}$ and light soak, depletion region and $E$-field are reduced permitting more $Cu^+$ ion diffusion toward the junction and the CdS. Though this level of Cu is still < 1% of the Cu near back contact region.

Figure 6-13. The band alignment of the TCO/CdS/CdTe/Cu/Au device structure taken from Corwin et al., 2004 [52].

6.7 Conclusion

The accelerated life testing experiments described in this chapter show that sputtered CdS/CdTe solar cells with 2.3 $\mu$m CdTe and 1-3 nm of Cu in the Cu/Au bilayer back contact exhibited the best stability when the devices received optimal CdCl$_2$ processing (~40 min at 387 °C). With 1-3 nm of Cu in the back contact, a fairly broad window of optimum CdCl$_2$ activation time at 387 °C is observed. CdTe cells with shorter treatment time produce higher defect and grain boundary density; by contrast the longer treatment introduce more Cl or S related defect states and thus yield larger degradation. Though CdTe cells without Cu at the back contact show poorer initial performance, the optimization range for chloride activation of these devices is wide. Increasing the Cu thickness beyond 3 nm leads to instability in the cells which is mainly dominated by FF and $J_{SC}$ loss. Much stronger Cu diffusion was observed on the cells with very thick Cu ($\geq 10$ nm) at back contact which primarily causes the cell degradation due to accumulation.
of large volume of Cu near junction. This effect might arise due to a decrease in built-in field and depletion region at $V_{OC}$ biasing condition. But when devices are stressed at short-circuit current or maximum power biasing conditions, CdTe cells have shown better stability [50, 57] inferring different behavior than $V_{OC}$ biasing.
Chapter 7

Influence of Sb$_2$Te$_3$ Back Contact on the Stability of Sputtered CdS/CdTe Solar Cells

7.1 Introduction

From Chapter 2 to Chapter 6, we have discussed several issues pertaining to sputtered CdS/CdTe cells contacted with evaporated Cu/Au. The discussion was mainly focused on optimization of fabrication parameters to achieve efficient cells with better stability. For completeness, we are looking for other contact materials (preferably Cu free) which could yield efficient and stable solar cells with sputtered CdTe films. Eventually, narrow band gap (~ 0.25 eV), p-type Sb$_2$Te$_3$ might be another appropriate option which was first used by Romeo et al. in 1999 [90]. This group has also reported that a bilayer Sb$_2$Te$_3$/Mo will be a very stable back contact for CdTe cells and has the capability to yield cell efficiency up to 15% [43, 44, 48, 90]. Similarly, other groups have identified the chemical stability of Sb$_2$Te$_3$ film when used as the back contact of CdTe solar cells [91, 92]. However, in recent years, high efficiency devices were not achieved consistently with Sb$_2$Te$_3$ as the contact material when other groups were trying to use it [93, 94].
We have chosen a step-wise approach to first study the growth properties, film morphology and the charge transport properties of Sb$_2$Te$_3$ films before directly contacting CdTe cells. We characterize the films using x-ray diffraction, four-point probe resistivity and Hall measurements. The deposition conditions for achieving the best films are then used for back contacts of sputtered CdS/CdTe solar cells. Finally, the stability of these solar cells with several back contacts using combinations of materials with Sb$_2$Te$_3$ (Sb$_2$Te$_3$/Mo, Au, Sb$_2$Te$_3$/Au, Sb$_2$Te$_3$/Cu/Au, Sb$_2$Te$_3$) are studied and the results are compared with our standard Cu/Au back contact devices.

7.2 Experimental

Sb$_2$Te$_3$ films were sputtered from a two-inch diameter target onto cleaned boro-alumino-silicate glass at substrate temperatures of nominally room temperature (RT), 100°C, 180°C, 210°C, 240°C and 270°C in an Ar ambient. The rf power and deposition pressure were fixed at 20W and 10 mTorr. The base pressure of the system was \(\sim10^{-6}\) Torr. As-grown films were mechanically scribed and the film thickness was measured by a stylus profilometer. Film thickness ranged from 0.48-0.7 \(\mu\)m with deposition rates of 3-4 Å/sec. Some films were annealed at 300°C, 325°C and 350°C for 30 minutes in vacuum.

The thin-film samples were analyzed with x-ray diffraction using the Cu-K$_{\alpha1}$ line \((\lambda = 0.154 \text{ nm})\) at 45 kV and 40 mA in the 0–20 geometry with instrumental resolution of 0.02 degrees. Hall measurements in the Van der Pauw configuration and resistivity measurements with a four-point probe were used to measure the electrical properties of the Sb$_2$Te$_3$ films. Finally, the best growth conditions were applied to prepare the back
contact of sputtered CdTe films. The accelerated life testing conditions described in Chapter 5 up to 300 hrs were used for stability studies.

7.3 Properties of Sb$_2$Te$_3$ Films

7.3.1 Growth Properties and Morphology

X-ray diffraction measurements, Figure 7-1, showed that all sputtered Sb$_2$Te$_3$ films were polycrystalline, except for the RT growth which was amorphous. Peak height increased with substrate temperature. The broad background for all samples is attributed to the aluminosilicate glass substrate. All crystallographic peaks shown in Figure 7-2(a) match the Sb$_2$Te$_3$ rhombohedral R-3m space group and are in good agreement with films grown using molecular beam epitaxy [95]. A peak at 20 = 17.5° [(0 0 6) plane] is the preferred growth orientation for substrate temperatures higher than 180 °C with best crystallinity at 240 °C. This suggests 240 °C as the best growth temperature for

![Figure 7-1. X-ray diffractogram of as-grown Sb$_2$Te$_3$ films sputtered at various substrate temperatures; a) RT, b) 100°C, c) 180 °C, d) 210°C, e) 240°C and f) 270°C.](image)
Figure 7-2. a) X-ray diffractogram of Sb$_2$Te$_3$ film grown at 240°C substrate temperature and subjected to 30 minutes post deposition heat treatment at 325 °C; b) Grain size of as-deposited Sb$_2$Te$_3$ films on boro-aluminosilicate glass vs. substrate temperature. Inset shows 30 minute annealing effects on the grain size of samples grown at 240 °C.
photovoltaic applications. The most prominent peaks are associated with the \(<0 0 3>\) crystallographic orientation. There is no indication of peak shift when as-grown films are heat treated. As shown in Figure 7-2(b), the grain size, as inferred from the peak width, of as-grown films increases with growth temperature which suggests improved crystallinity at higher temperature growth but the post-deposition heat treatment does not increase grain size (see in inset Figure 7-2(b)).

### 7.3.2 Charge Transport Properties

In order to quantify electrical properties such as resistivity, carrier concentration and mobility, Hall measurements were made using the Van der Pauw configuration. As shown in Figure 7-3, excellent agreement was obtained between the four-point probe and Hall measurements. The carrier concentration, shown in Figure 7-4(a), remains fairly constant with increasing deposition temperature until 240 °C and then increases substantially for 270 °C. The mobility improves monotonically with substrate temperature before dropping at 270 °C. The XRD results indicate that the \(\text{Sb}_2\text{Te}_3\) films increase in grain size up to 240 °C. The increase in grain size would reduce interface scattering of the charge carriers and explain the higher mobility for higher temperature depositions [96]. At 270 °C the grain size increases further and the carrier concentration triples. The factor of two decrease in the Hall mobility at 270 °C is due to an increase in ionized impurity scattering.

Qualitatively similar behavior occurs with post-deposition annealing of films deposited at 240°C. The mobility improves with post-deposition heat treatment at 300 and 325 °C as shown in Figure 7-4(b). But the mobility drops with annealing at 350 °C as the carrier concentration rises, again consistent with ionized impurity scattering.
However the carrier concentration after 350 °C annealing is still a factor of two less than that achieved by deposition at 270 °C.

Figure 7-3. Comparison of resistivity vs. growth temperature of as-grown Sb$_2$Te$_3$ films using two different techniques.

### 7.4 Sputtered CdTe Cells With Cu-free Back Contacts (t = 0 hrs)

Sputter deposition at 240 °C was chosen for deposition of the Sb$_2$Te$_3$ back contacts to sputtered CdTe cells. The CdTe cells were fabricated as described in Section 2.2 with the structure glass/SnO$_2$:F/HRT/CdS (80 nm)/CdTe (2.1 μm) followed by 35 minutes CdCl$_2$ treatment at 387 °C in dry air and rinsed with methanol. Several different back contact structures were used for comparison. Sb$_2$Te$_3$ (100-500 nm), Cu (3 nm)/Au (20 nm) and/or Mo (900 nm) were either sputtered (Sb$_2$Te$_3$, Mo) or thermally evaporated (Cu, Au) onto the CdTe layer through a metal mask.
Figure 7-4. Hall mobility and carrier concentration of Sb$_2$Te$_3$ films measured in the Van der Pauw configuration; a) as-grown and b) annealed films grown at 240 °C.

All CdTe cells using Cu in the back contacts were diffused at 150°C for 45 minutes before the J-V and QE measurements. As shown in Figure 7-5, Cu contacted
devices had 2-3% higher efficiency than cells without Cu at the back contact. The spread in efficiency of these cells demonstrated very tight distributions. Unlike Cu-contacted cells, Cu-free devices exhibited higher series resistance which causes 10-15% loss in fill factor. Moreover, 100-200 mV lower $V_{OC}$ was also observed on such cells probably due to inadequate p-type doping at the contact side. Note that even when a very small amount of Cu (1-3 nm) is deposited after the $\text{Sb}_2\text{Te}_3$, the $V_{OC}$ improves substantially to nearly that of the Cu/Au contact. The back contacts with Au only, $\text{Sb}_2\text{Te}_3$/Au or $\text{Sb}_2\text{Te}_3$/Mo also have reverse-diode behavior as seen in the distinct roll-over in quadrant one and do not reach the efficiency of the Cu/Au back contact, Figure 7-6(a).

![Box and whisker plot of efficiency of CdS/CdTe solar cells with six different back contact combinations.](image)

**Figure 7-5.** Box and whisker plot of efficiency of CdS/CdTe solar cells with six different back contact combinations. Thin-film CdTe devices were prepared with identical cell processing parameters before back contact applications. Devices finished with Cu in contact layer (left two samples) were diffused at 150 °C for 45 minutes in room ambient [Note: 25 dot cells were plotted for each back contact. The upper and lower limits of the box and whisker symbol are 75-25% and 95-5% respectively.]
Table 7.1: Performance indicators of the best CdS/CdTe cells with six different back contact structures. The Cu/Au (3 nm/20nm) is UT’s standard for back contact comparison.

<table>
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<th>Back contacts</th>
<th>$V_{OC}$ (mV)</th>
<th>$J_{SC}$ (mA/cm$^2$)</th>
<th>FF (%)</th>
<th>$\eta$ (%)</th>
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<td>21.4</td>
<td>75.6</td>
<td>13.2</td>
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<tr>
<td>500 nm Sb$_2$Te$_3$+ 3 nm Cu + 20 nm Au</td>
<td>778</td>
<td>22.1</td>
<td>71.8</td>
<td>12.3</td>
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<tr>
<td>100 nm Sb$_2$Te$_3$+ 20 nm Au</td>
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<td>22.2</td>
<td>63.2</td>
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</tbody>
</table>

The unbiased quantum efficiencies of the best cells shown in Figure 7-6(a) are plotted in Figure 7-6(b). Normally, for Cu contacted cells the short wavelength collection is larger than for wavelengths near CdTe band edge so that a slope at 600-800 nm can be observed in the QE data. In contrast, the CdTe cells without Cu at the back contact have shown a plateau shaped QE which implies lower collection near the CdS/CdTe junction might be related to poor doping concentration due to absence of Cu.

7.5 Stability of Sputtered CdTe Cells With Cu-free Back Contacts

(t = 300 hrs)

Light soaking tests up to 300 hrs under the conditions described in Chapter 5 were applied to the CdTe solar cells with the six different back contacts described in Table 7.1. Box and whisker plots of the data are shown in Figure 7-7(a) for 25 dot cells with each type of back contact before and after 300 hours of light soaking. The initial and final spread of cell efficiencies is higher for all contacts other than Cu/Au but we suspect that this is due partly to inadequate optimization of the new contact structures and processes.
Figure 7-6. a) Light J-V and b) quantum efficiencies of the sputtered CdS/CdTe cells finished with six different back contacts presented in Table 7.1.

After ALT, CdTe cells with Sb$_2$Te$_3$/Mo contacts exhibited less fractional change than the cells with back contacts of Sb$_2$Te$_3$/Au or Sb$_2$Te$_3$ alone. Lower fill factor and lower short-circuit current was observed in these devices which might be related to the
oxidation of antimony and the resulting increase in the series resistance. Since the solar cells with the Au-only contact were not diffused at 150 °C after the deposition, an improvement after light soaking was observed as expected. During 300 hrs light soaking stress Au diffuses into CdTe and forms better contact.

Representative current-voltage characteristics of Cu/Au and Sb$_2$Te$_3$/Mo contacted CdTe cells are shown in Figure 7-7(b). After 300 hrs light soaking, both types of devices have shown reasonable stability. We observed fractional change in $V_{OC}$ for Cu/Au contacted cell (as explained in Chapters 5 and 6) where Sb$_2$Te$_3$/Mo contacted cell had $J_{SC}$ loss. The cells with Sb$_2$Te$_3$/Mo contacts, showed weaker roll-over effects after stressing than initial measurement indicating a lower contact resistance was formed between CdTe/Sb$_2$Te$_3$ interface.

### 7.6 Conclusion

Sputter deposition of Sb$_2$Te$_3$ films on glass was optimized with x-ray diffraction, and Hall-effect measurements prior to using it for a back contact material for CdTe cells. The optimized sputter process at 240°C was used to fabricate a variety of CdS/CdTe back contacts incorporating a layer of Sb$_2$Te$_3$. The CdS/CdTe cells completed with back contacts that used Sb$_2$Te$_3$ layers achieved efficiencies in the range of 9 – 12%, which was 1% to 4% lower than the best Cu/Au back contacts. The use of 3 nm of Cu after the Sb$_2$Te$_3$ yielded performance nearly as good as Cu/Au with a similar amount of Cu.
Figure 7-7. a) Efficiency comparison of CdS/CdTe solar cells with various back contacts before and after ALT tests. Solar cells were light soaked without encapsulation under one-sun illumination at 85 °C, open-circuit biasing in room ambient for 300 hrs. [Note: 25 dot cells were used for each back-contact material. The upper and lower limits of the box and whisker symbol are 75-25% and 95-5% respectively.] b) Light J-V of the best cells for two different back contacts at t = 0 hrs (solid line) and t = 300 hrs (dashed line).
After 300 hours of accelerated light soaking, CdTe solar cells with Sb$_2$Te$_3$/Mo back contacts are as stable as Cu/Au back contacts. Further continuation of this study may provide greater latitude in achieving better efficiency as well as the stable performance under accelerated life testing conditions.

In UT standard cell fabrication process, we do not apply chemical etching before back contact deposition. Since the roll-over effect was observed on Cu-free back contacts, it could be due to oxidation of contacted materials. We believe a very short etching process may improve the contact resistance and hence increase the cell performance.
Chapter 8

Influence of High Temperature Activation on the Stability of Sputtered CdS/CdTe Solar Cells

8.1 Introduction

In the previous chapters, we mostly discussed the cell fabrication parameters that can explicitly affect the stability of sputtered CdS/CdTe cells. But the research in this chapter is focused on a different approach. In Chapter 6, we found that CdTe devices need 25-40 minutes of CdCl$_2$ treatment at 387 °C to achieve better efficiency as well as stability. But with a long activation step, it would not be cost-effective for high-speed production. Therefore, a short chloride activation process is generally advantageous for industry. Here we explore a short activation process using higher temperatures (>400 °C) sometimes this is called a “rapid thermal process” or RTP. We compare the cell performance and the resulting cell stability with our regular treatment process.

The second approach of this chapter is an extension of stability study of Chapter 5 using international standards. The testing conditions we use here are more closely related to standards in the industry such as UL 1703 and IEC 61646 [97]. One of these is an environmental test involving damp heat where solar cells are held at 85 °C with 85%
relative humidity. In this experiment, the effects of temperature and humidity on CdTe cells are studied. The second test is again light soaking. The outcomes of the both tests will be compared. For this study, we again start with sputtered CdS/CdTe cells finished with UT’s standard fabrication process as described before.

8.2 Experimental

Standard CdS/CdTe films were sputtered on Pilkington standard HRT-coated TEC15 glass substrates as described in Section 2.2. After application of the CdCl₂ solution, the as-grown CdS/CdTe films were held between a pair of thin graphite susceptors (~1/4” thick) with a variation in activation temperature (370 °C, 390 °C, 400 °C, 410 °C, 430 °C and 440 °C) and treatment time. Because of the Arrhenius behavior of the S and Cl diffusion [30], the treatment times were reduced for the higher temperatures. After treatment, CdTe samples were cooled down quickly to room temperature with the help of extra N₂ flow. The treated films were characterized using x-ray diffraction to confirm the optimum re-crystallization and intermixing. Finally, standard Cu/Au contacts were applied to the treated films. About 20-25 dot cells for each treatment condition were prepared. The baseline efficiency of these cells is well above 12% with our standard fabrication.

The complete device structures then received either light soaking tests or environmental tests for a continuous 300 hrs. The light soaking test used similar conditions as described in Chapter 5. For the damp heat test, CdTe samples were exposed at a constant 85 ± 0.1 °C and 85± 0.1 % RH with an open-circuit biasing inside
a Cincinnati Sub-Zero EZT-560 environmental chamber. The J-V measurements were carried out before and after the stress.

8.3 Activation Temperature vs. Cell Performance

In this section, we explain the optimization of high-temperature chloride activation process on the basis of cell performance. For this, we treated the cells with three different treatment times for each activation temperature. To select the optimum chloride activation, the best efficiency as well as the best yield condition was chosen. For example, at 430 °C, devices received 1 minute, 3 minutes and 10 minutes treatment times at maximum temperature ($T_{max}$). Among them, 3 minutes produced the highest efficiency cells with the better yield and we picked this as an optimum treatment time. Likewise at 440 °C, about 20 seconds treatment time yielded the better efficiency. The performance parameters of these cells treated at 430 °C and 440 °C are compared at Table 8.1.

The current-voltage characteristics of the cells shown in Table 8.1 are plotted in Figure 8-1(a) and 8-1(b). As expected, comparatively higher $J_{SC}$ was realized for longer treatment time indicating stronger S diffusion but that leads to more defect states in CdTe and results lower $V_{OC}$ and FF. With optimal treatment time, CdTe cells exhibited nearly 13% average efficiency when the activation temperature was held at 370 °C but at higher temperature the efficiency decreased to 11.3%, Figure 8-2. This might be related to poorer junction properties as well as poor electrical properties of CdTe due to rapid diffusion at the higher temperature. Above 400 °C activation temperature, the solar cells showed relatively poorer FF and $V_{OC}$ than lower-temperature treatment conditions although the $J_{SC}$ of these cells are comparable. The treatment time vs. activation temperature plot (Figure 8-2) shows an exponential relation suggesting an inverse Arrhenius behavior of treatment time which will be discussed more details in Section 8.5.
Figure 8-1. Current-voltage characteristics of the sputtered CdTe cells activated for three different treatment times at; a) 430 °C and b) 440 °C.
Figure 8-2. Cell efficiency vs. activation temperature of thin-film CdTe devices. A variation in optimum treatment time which was measured at maximum temperature ($T_{\text{max}}$) with activation temperature is shown on right scale which drops off exponentially. The data points for 380 °C and 420 °C are interpolated in the graph which are not observed directly.

Table 8.1: Performance indicators of sputtered CdTe cells with high temperature activation conditions. [Note: Bold denotes the optimum treatment time for that particular temperature.]

<table>
<thead>
<tr>
<th>Activation temperature (°C)</th>
<th>Treatment time at $T_{\text{max}}$ (min.)</th>
<th>Cell performance parameters</th>
<th>$V_{\text{oc}}$ (mV)</th>
<th>$J_{\text{sc}}$ (mA/cm$^2$)</th>
<th>FF (%)</th>
<th>Eff (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>430</td>
<td>1</td>
<td></td>
<td>804</td>
<td>23.5</td>
<td>65.4</td>
<td>12.4</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td></td>
<td>823</td>
<td>22.6</td>
<td>69.8</td>
<td>13.1</td>
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<td></td>
<td>787</td>
<td>22.9</td>
<td>67.7</td>
<td>12.2</td>
</tr>
<tr>
<td>440</td>
<td>0.33</td>
<td></td>
<td>788</td>
<td>23.4</td>
<td>64.3</td>
<td>11.9</td>
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<td>3</td>
<td></td>
<td>737</td>
<td>24.3</td>
<td>63.8</td>
<td>11.4</td>
</tr>
</tbody>
</table>
8.4 X-ray Diffraction of High-temperature Activated CdTe Films

The optimal chloride activation that was estimated in Section 8.3 is further confirmed by x-ray diffraction. For this, we performed x-ray diffraction (XRD) of all six different samples in a wide angle scan from 21° to 80° at ~0.02° steps. The diffractogram of three representative samples presented in Figure 8-3(a) shows that treated films were almost randomly oriented after CdCl$_2$ activation; however, the sample treated at 440 °C received only 20 seconds treatment time. The intensity of the XRD profile for each temperature is comparable whether the treatment was done at 370 °C, 410 °C or 440 °C.

With the XRD data, we also observe sufficient intermixing of CdS and CdTe layers as described by McCandless et al. [36]. A narrow-angle scan was performed across the (511) peak profile (Figure 8-3(b)) that estimates about $x \sim 0.02$ alloying of CdS$_x$Te$_{1-x}$ for all treatment temperatures. As explained in Chapter 3, this implies nearly optimum treatment time for sputtered CdTe cells. The secondary peak with the longer shoulder on the high angle side of the profile corresponds to the alloy with greater intermixing. On the basis of these observations, the CdTe film activated at 410 °C exhibited slightly $> 0.02$ sulfur content is considered to be little bit overtreated.
Figure 8-3. X-ray diffraction of sputtered CdS/CdTe films on HRT-coated SnO$_2$:F glass substrates received nearly optimum CdCl$_2$ activation at three different treatment temperature; a) wide angle XRD and b) high angle XRD profile along (511) direction.
8.5 Optimum CdCl₂ Activation at High Temperature

When a CdTe sample receives CdCl₂ treatment at higher temperature, the time spent ramping up and cooling down will be significant. Here, we define a *nominal treatment time* which includes a small correction on our regular treatment time that used to be measured at maximum temperature ($T_{\text{max}}$). The new treatment time includes both ramp up and cool down period above 350 °C which is the minimum temperature required for chloride activation as suggested by Mccandless & Sites 2003, [14]. As shown in Figure 8-4, the activation time measured at 430 °C is 2.5 minutes which is recorded at maximum temperature [Line BC]. But when the CdTe sample is in the heating [Line AB] and cooling [Line CD] stages, some reaction and diffusion occurs, albeit more slowly. Therefore, a new treatment time is defined which is line ABCD in Figure 8-4, and called the *nominal treatment time*. As described in Section 8.3, we first optimized our regular

![Figure 8-4](image-url)  
**Figure 8-4**: A typical temperature profile of a CdCl₂ activation done at 430 °C.
activation time on the basis of cell performance and then converted it into *nominal activation time* by using temperature profile for each activation condition. The best treatment conditions for each temperature on the basis of sputtered cell performance are given in Table 8.2.

**Table 8.2:** Activation temperature vs. optimum treatment period. The *nominal treatment time* given in third column includes ramp up and cool down period at 350 °C or higher temperature. [**To minimize the effects of other cell parameters, only six samples from a 3” X 3” plate were possible which did not include 380 and 420 °C activation condition.**]

<table>
<thead>
<tr>
<th>Activation temperature</th>
<th>Treatment time at $T_{\text{max}}$ (min.)</th>
<th>Nominal treatment time (min.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>440 °C</td>
<td>0.33</td>
<td>3</td>
</tr>
<tr>
<td>430 °C</td>
<td>2.5</td>
<td>5</td>
</tr>
<tr>
<td><strong>420 °C</strong></td>
<td>-</td>
<td>9</td>
</tr>
<tr>
<td>410 °C</td>
<td>12</td>
<td>14</td>
</tr>
<tr>
<td>400 °C</td>
<td>20</td>
<td>22</td>
</tr>
<tr>
<td>390 °C</td>
<td>31.5</td>
<td>33</td>
</tr>
<tr>
<td><strong>380 °C</strong></td>
<td>-</td>
<td>51</td>
</tr>
<tr>
<td>370 °C</td>
<td>79</td>
<td>80</td>
</tr>
</tbody>
</table>

**8.5.1 Estimation of Activation Energy ($E_a$)**

In this section, we present a calculation to estimate the activation energy by using *nominal time* from Table 8.2. For this, a graph of nominal activation time (in log scale) vs. inverse temperature (in 1000/T K$^{-1}$) is plotted in Figure 8-5.

According to the kinetic theory of diffusion, for one-dimensional diffusion from a source of constant concentration there is a characteristic diffusion length $l = 2\sqrt{D(T)t}$ ;
Figure 8-5. Nominal treatment time vs. treatment temperature of sputtered CdTe cells processed with high temperature activation [Note: Logarithmic scale in Y-axis, the data points are taken from 3rd column of Table 8-2 and red dotted line is a straight line fit.]

where ‘D’ is the diffusion coefficient and ‘t’ is the diffusion time [4]. For a constant diffusion length such as the CdTe thickness (~2 μm), the diffusion time can be expressed as:

\[ t \propto \frac{1}{D(T)} \] .......................... (8.1)

The diffusion coefficient typically has an “activated” behavior can be written as:

\[ D(T) = D_o \exp\left(\frac{-E_o}{K_B T}\right) \]

\[ \Rightarrow t = \frac{C_o}{\exp\left(\frac{-E_o}{K_B T}\right)} \] .......................... (8.2)
Where ‘$K_B$’ is the Boltzmann constant and ‘$T$’ is the activation temperature, ‘$E_a$’ is the activation energy and ‘$C_o$’ is a proportionality constant depending on the material properties of diffusion length and thickness of the film. After taking the natural log on Eqn (2) we obtain,

$$\ln(t) = \frac{E_a}{K_B T} + \ln(C_o) \hspace{1cm} \text{..........................} \quad (8.3)$$

Now the slope of the straight line $\ln(t)$ vs. $(1/T)$ would be ‘$E_a/K_B$’. If we consider the nominal activation time is the net diffusion time, this slope is equivalent to the slope we calculated in Figure 8-5. Therefore,

$$\frac{E_a}{K_B} = 21.414 \times 1000 \hspace{1cm} \text{..........................} \quad (8.4)$$

$$\Rightarrow E_a = 1.78 \pm 0.05\text{eV}$$

Where $K_B = 8.617 \times 10^{-5}$ eVK$^{-1}$, and the error in activation energy is estimated by least square fit from origin.

McCandless et al. [30] and Lane et al. [98] reported that the activation energy for grain boundary diffusion of sulfur (in the presence of CdCl$_2$) into CdTe is about 1.9-2.0 eV. With our assumptions, the calculation shows relatively close agreement with this reported value. Kaur, et al. [99] suggested that activation energy for diffusion process in polycrystalline materials also depends on the size of grain boundary indicating that it can vary accordingly when grains are loosely or tightly bounded. For 2 $\mu$m thick CdTe device, Y-intercept of the straight line fitting from Figure 8-5 results:

$$C_o = (1.8 \pm 0.1) \times 10^{-3} \text{ (cm}^2/\text{s})^{-1} \hspace{1cm} \text{..........................} \quad (8.5)$$
Therefore, the inverse Arrhenius behavior (Eq\(^2\)) of the nominal treatment time is expressed as:

\[
t = \frac{(1.8 \pm 0.1) \times 10^{-3}}{\exp\left(\frac{-1.78 \pm 0.05}{K T}\right)} \quad \ldots \ldots \ldots (8.6)
\]

### 8.6 Accelerated Life Testing (t = 300 hrs)

#### 8.6.1 Stability of RTP Cells Under ALT

The stability of CdTe cells that received high-temperature activations (treated at 440 °C and 430 °C) were compared with regular CdTe devices after both 300 hrs light soaking (LS) and damp heat (DH) tests. Unlike regular devices, CdTe cells activated at higher temperature showed anomalously improved FF and \(V_{OC}\) without losing the short-circuit current during either LS or DH stress. An average of 65% fill factor and 780 mV open-circuit voltage was measured before ALT, Figure 8-6(a) and 8-6(b). After 300 hrs LS and DH test, the average performance is increased substantially to well above 70% and 820 mV respectively.

Compared with damp heat test, light-soaked cells exhibited more improvement indicating that the one-sun illumination is highly advantageous for improving the cell performance. It should be noted that the lower initial performance achieved on sputtered cells might be related to short period high-temperature activation.

Although sputtered CdTe cells activated at higher temperature show poorer initial performance, they ended up with better efficiency (especially after light soaking test) than devices with the standard chloride treatment, shown in Figure 8-7. After accelerated
Figure 8-6. Box and whisker plots of; a) fill factor and b) open-circuit voltage of the CdTe cells that received various chloride activation treatments and different ALT conditions. About 25 dot cells were plotted for each ALT condition.
life testing, we might think there is a significant reduction in the density of defect states such that the CdTe devices then exhibited better electrical properties and improved FF and \( V_{OC} \). Further study is needed to confirm these interferences which will be also helpful to understand the micro-structural changes that occur during high temperature activation and ALT.

![Figure 8-7](image)

**Figure 8-7.** Efficiencies of sputtered CdTe cells the received different chloride activation treatments before and after accelerated life testing of either damp heat (DH) or light soak (LS). About 25 dot cells were plotted for each ALT.

### 8.6.2 Light Soaking vs. Damp Heat

Herein, we are further interested to observe the stability under damp heat where the CdTe cells are prepared with or without polymer encapsulation and compare the results with light-soaked samples. The encapsulation method we used is a simple vacuum seal with a food-saver plastic bag. For this test, sample 249-I was enclosed inside a 2” diameter non-sealing fluoroware polymer box similar to that used for semiconductor
wafers. After adding some silica gel desiccant and CaCl$_2$ indicator outside the sample box, the fluoroware box was vacuum sealed into a standard food-saver plastic bag. The sealed sample (249-I) and a bare sample (249-II) were held in the damp heat test for 300 hrs. After continuous stress, the desiccant inside the sealed plastic had changed its color indicating that there had been significant moisture ingress; however, the bag still showed evidence of a good vacuum seal, shown in Figure 8-8.

![image](image)

**Figure 8-8.** CdTe sample inside fluoroware container sealed inside plastic bag together with silica desiccant/CaCl$_2$ indicator; a) before and b) after 300 hrs of damp heat test.  
[**Note:** Color difference is due to camera auto color balance. Polymer did not significantly yellow.]

The $V_{OC}$, $J_{SC}$, FF and efficiency of CdTe cells (at least 10 cells for each test) measured before and after 300 hrs continuous stress are respectively shown in Figure 8-9(a) to Figure 8-9(d). Both sealed and bare samples, 249-I and 249-II, showed *improvements* in efficiency of a 10-20 mV $V_{OC}$ and 1-2% FF increment where $J_{SC}$ remained same within experimental error suggesting almost no effects of humidity on sputtered CdTe cells. We expected to see oxidation effects on Cu and a loss in FF. But
the result was opposite and our prediction failed when no influence of humidity was observed on 3 nm Cu which was capped by 20 nm Au from outside.

![Box and whisker plots](image)

**Figure 8-9.** Box and whisker plots of; a) open-circuit voltage b) short-circuit current, c) fill factor and d) efficiency of the sputtered CdTe cells that received various ALT conditions. About 10-25 dot cells were plotted for each stressing condition.

Unlike damp heat cells, light-soaked sample (249-III) which was not sealed inside food-saver plastic bag showed comparable efficiency before and after stress; however, this set of devices had variations in FF, J_{SC} and V_{OC}. These cells were also started with little lower initial performance than damp heat cells.
8.7 Conclusion

Sputtered thin-film CdS/CdTe cells activated at higher temperature (>400 °C) have exhibited somewhat lower efficiency than the regular devices. We believe the very short activation time, which includes quick ramp up and cool down process, forces rapid diffusion of Cl and S into CdTe. This may introduce some defect states in CdTe such that the treated film shows slightly poorer electrical properties. These devices have shown relatively lower FF and \( V_{OC} \). On the basis of cell performance, we optimized the treatment condition and determined the activation energy \( 1.78 \pm 0.05 \text{ eV} \) which is in close agreement to the value reported by McCandless et al. [30] and Lane et al. [98] for grain-boundary diffusion of S in CdTe in presence of CdCl\(_2\). A substantial improvement in cell performance is observed on these devices when they received 300 hrs of light soak or damp heat perhaps due to some recovery in electrical properties. On the other hand, sputtered CdTe cells demonstrated no loss after 300 hrs stressed in damp heat condition inferring no direct evidence of humidity effect in our typical device structure.
Chapter 9

Summary and Future Work

9.1 Summary

We used magnetron sputtering to deposit CdS and CdTe layers on Pilkington SnO$_2$:F coated glass substrate coated with a highly resistive transparent layer. The fabricated CdS/CdTe cell structures after standard CdCl$_2$ activation and Cu/Au contacts exhibited efficiency over 13.5%. With proper optimization of post-deposition processing, we achieved the highest efficiency, ultra-thin cells ever reported which showed over 8% efficiency for 0.25 μm, 11% efficiency for 0.5 μm and 12.5% efficiency for 0.75 μm CdTe thickness. We found that the lower efficiencies obtained on such ultra-thin devices are mainly due to loss in photon absorption. We modeled this deep penetration loss of short-circuit current as a function of absorber layer thickness using the known absorption coefficient of CdTe.

CdS/CdTe cells that received high temperature annealing at 450 °C in dry air without CdCl$_2$ exhibited over 11% efficiency. This is significant because without chlorine, the grain boundaries of sputtered films are not expected to passivate well and the devices show poorer electrical properties. Further characterization of these devices
with the help of secondary electron microscopy and x-ray diffraction confirmed sufficient re-crystallization and alloying of the CdS\(_{x}\)Te\(_{1-x}\) layer which is required for high efficiency cells. But without chlorine, these devices did not show complete grain boundary passivation so that an additional short (5 minute) CdCl\(_2\) activation at 400 °C improved \(V_{OC}\) by 30-50 mV and FF by 2-5%.

This dissertation also characterized thin-film Sb\(_2\)Te\(_3\) as a potential back contact (BC) material for CdS/CdTe solar cells. Several types of BCs incorporating Sb\(_2\)Te\(_3\) were applied on sputtered CdS/CdTe cells; however, none of the devices reached the efficiency of our standard Cu/Au contacts. We did find that depositing a small amount of Cu after the Sb\(_2\)Te\(_3\) enhanced the \(V_{OC}\) and FF by 20% indicating that Cu is still a key factor of doping the CdTe for sputtered cells when Sb\(_2\)Te\(_3\) is used.

The main goal of this dissertation was to find out the primary causes that affect the long-term stability of magnetron-sputtered CdS/CdTe cells. We performed accelerated life testing (ALT) on cells prepared by varying several parameters such as substrate types, CdS thickness, CdTe thickness, CdCl\(_2\) activation and Cu thickness. The sputtered CdTe cells exhibited less than 5% relative loss in efficiency after 900 hrs of light soaking under one-sun illumination, without encapsulation, at 85 °C, with open-circuit voltage biasing, in room ambient when processed with optimal parameters. The stability of these devices was more sensitive to the CdCl\(_2\) activation and Cu thickness than to the CdS and CdTe thicknesses. We also noticed that the stability was independent of the substrate type; however, HRT-coated substrates have a slight advantage in the cell performance when a very thin CdS layer is used. The open-circuit voltage (\(V_{OC}\)) and fill factor (FF) were the parameters most important to cell stability. On the other hand, short-
circuit current ($J_{SC}$) was not affected except for very thin CdS or CdTe devices. After optimization, CdTe cells sputtered on HRT-coated TEC15 substrates with 100 nm CdS, 2.1 µm CdTe, and 30 minutes of chloride activation at 387 °C, 3 nm Cu, 20 nm Au followed by a 45 minute diffusion at 150 °C showed excellent stability. In addition to our standard Cu/Au back contact, Sb$_2$Te$_3$/Mo was found to be a stable Cu-free back contact material for sputtered cells but the efficiency of these devices was about 10% which is much lower than Cu/Au contacted cells (13.5%).

Secondary ion mass spectroscopy (SIMS) data which was performed at NREL did not show any evidence of Cu diffusion of light-soaked cells after 300 hrs when 3 nm Cu is used at the back contact. But a 10 nm Cu produced significantly increased Cu concentration near CdTe/CdS junction side and degraded the cells up to 60% indicating that Cu is detrimental to the cell stability when too much is used. SIMS data also confirmed the migration of S, Cl and O into CdTe after chloride activation but remained unaltered after 300 hrs of light soaking.

Furthermore, the effect of short-time-duration, high-temperature activation on sputtered CdS/CdTe cells was studied. Devices activated above 400 °C showed relatively lower efficiency than the cells treated below 400 °C indicating that rapid diffusion of S (or Cl) is not favorable to the sputtered devices. We identified an inverse Arrhenius dependence on activation time from which we estimated about 1.78 ± 0.05 eV activation energy for S diffusion into sputtered CdTe film in the presence of CdCl$_2$. After receiving 300 hrs of light soaking or damp heat (85 °C /85% RH) stress, CdTe cells activated at higher temperature (430 °C and 440 °C) showed an improvement up to 20% in relative measurement but the improvement mechanism has yet to be understood.
In addition, under damp heat, unencapsulated standard sputtered CdTe cells survived with essentially no performance loss after 300 hrs of stress implying that 20 nm of Au is more than enough to cap the 3 nm Cu layer in cells prepared by our sputter deposition process.

9.2 Future Work

As explained in Section 9.1, we successfully fabricated sputtered cells for a wide range of CdTe thicknesses with various CdCl₂ activation conditions and studied their stability. With these results, we would like to propose some further work related to sputtered CdTe cells for future prospects that may provide more information to further improve the cell performance as well as the long-term stability. The following are some suggestions:

1. We tested the stability of CdTe cells under $V_{OC}$ biasing which is the most convenient way when many devices are used. But real-world solar cells operate at the maximum power point. Therefore, extended stability studies of sputtered cells at different biasing conditions would be more relevant.

2. To protect from environmental effects, thin-film solar modules are always encapsulated while operating in the field. Therefore, an extension of ALT studies with encapsulated sputtered devices needs to be done.

3. In addition to light-soaking and short-period damp-heat stress, there are international standards to certify solar modules that involve other ALT stresses including thermal cycling (TC200), humidity-freeze, damp heat (DH1000). We
believe these tests are more important when devices are encapsulated. Thus, further study of encapsulated cells with these tests should be done.

4. Thin-film solar modules are monolithically interconnected with the application of laser scribing. But this isolation technique will result some dead area in the solar panels such that devices show different series resistance behavior than laboratory device structures. Therefore, using such types of monolithically integrated mini-modules in stability tests needs to be done.

5. This work has shown that ultra-thin CdS/CdTe cells with CdTe thickness of less than 0.5 µm can have high performance. We believe that these studies of ultra-thin CdTe cells should be extended to include 1 mm thick aluminosilicate glass substrates which have higher optical transparency.

6. We also suggest that the use of a very thin back buffer layer between CdTe and back contact [64] in ultra-thin device structures will further improve the device performance.

Besides these, there are many other ways to improve the cell performance and long-term stability of CdTe cells such that this thin-film technology can be established as the best, low-cost photovoltaics in the future solar market. Among them, improvement in open-circuit voltage, exploration of cheap and stable back contact materials, substrate configuration are global issues.
References


69. Xiangxin Liu, private communication.


