Modelling of GaN power switches

Sreeram Jogi
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A Thesis

entitled

Modelling of GaN Power Switches

by

Sreeram Jogi

Submitted to the Graduate Faculty as partial fulfillment of the requirements for

the

Master of Science Degree in

Electrical Engineering

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The University of Toledo
August 2015
An Abstract of

Modelling of GaN Power Switches

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The main goal of this work was to develop the necessary expertise and model various parameters and characteristics of gallium nitride power HEMT (High Electron Mobility Transistor) devices. These include modelling of voltage-current characteristics, high temperature reverse bias leakage current, some circuit simulation, as well as radiation related effects on the device performance.

Before modelling gallium nitride transistors, several other types of devices were modelled as part of a process to better understand the underlying physics involved in simulating HEMTs.

To better compare the performance of commercially available gallium nitride transistors with the modelled gallium nitride devices, different types of depletion and enhancement structures of gallium nitride transistors were modelled. The voltage-current characteristics are simulated for various physically modelled gallium nitride structures. The obtained results are
compared with those for commercially available gallium nitride transistors. Furthermore, drain to source leakage currents (at high temperature) of physically modelled gallium nitride devices were also modelled and are compared with performance of commercially available gallium nitride devices such as from Efficient Power Conversion Corporation (EPC®), including with actual measurements and test performed in our lab. The resulting simulations and experiments gave insight towards the factors which were limiting the device performance due to self-heating, leakage currents and the device geometry.

We reviewed the electrical behavior of AlGaN/GaN HEMTs using circuit simulation tools. Basic power circuits were modelled in PSpice® (Circuit simulator from OrCAD Cadence) and Silvaco TCAD® (Process & Device simulator framework from Silvaco, Inc.), in order to observe switching behavior and compare the obtained results. To do this, commercially available EPC 2012 devices were imported into PSpice® and physically modelled enhancement gallium nitride HEMT devices were imported into MixedMode® (Circuit simulation module in Silvaco TCAD®). Additionally, experimental switching results are also discussed.

The degree of immunity to single event effects such as heavy ion radiation is simulated and compared using ATLAS® (Device simulation module in Silvaco TCAD®). Also, an effect of long-term switching (latching) in both the off- and on-state, in unpackaged devices exposed to blue laser light, was experimentally
observed in our lab. To understand this latching effect, in a simulated gallium nitride device, a layer of (trapped carrier) charge was assumed to form as a result of the irradiation. To model this behavior, a substantial amount of interface charge is added to the device and simulations were able to replicate the observed latching effect. This experiment demonstrates that trap-related light absorption and charge carrier generation plays a major role in the device performance.
This thesis is dedicated to my parents, for their unconditional love, encouragement and support. Thank you for everything.
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I am really fortunate in having enormous support and insightful comments from my family, advisors, friends and colleagues. I couldn’t have done without your help and suggestions.

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List of Abbreviations

2DEG ...................... Two-Dimensional Electron Gas

AlGaN ..................... Aluminum Gallium Nitride

BJT ........................ Bipolar Junction Transistor

DUT ......................... Device under Test

FET .......................... Field Effect Transistor

GaAs ........................ Gallium Arsenide
GaN .......................... Gallium Nitride

HEMT ........................ High Electron Mobility Transistor

JFET ........................ Junction Field Effect Transistor

MESFET ...................... Metal Semiconductor Field Effect Transistor
MOSFET ...................... Metal Oxide Semiconductor Field Effect Transistor

PPE .......................... Piezo-Electric Polarization
PSP ........................... Spontaneous Polarization

SEB .......................... Single Event Burnout
SEE .......................... Single Event Effect
SEGR .......................... Single Event Gate Rupture
SEU .......................... Single Event Upset
Si .............................. Silicon
SiC ............................. Silicon Carbide

VDS .......................... Drain-Source Voltage
VGS .......................... Gate-Source Voltage
VTH .......................... Threshold Voltage
List of Symbols

\( \mu \) .........................Micro
\( n \) ............................Nano
\( p \) ..............................Pico
\( \psi \) ..............................electrostatic potential
\( \varepsilon \) .........................permittivity
\( \rho \) .............................space charge density
\( G_n \) ..............................generation rates of electrons
\( G_p \) ..............................generation rates of holes
\( J_n \) ..............................electron current density
\( J_p \) ..............................hole current density
\( K \) .................................Degrees in Kelvin
\( R_n \) ..............................electron recombination rate
\( R_p \) ..............................hole recombination rate
Chapter 1    Introduction

1.1 Background of Switching Power Transistors

In an electrical circuit, a switch is a three terminal device that controls the line terminals electrical potential using a control terminal. Electromechanical devices called relays are among the first version of switches which were used to control electrical connections. It was not until early twentieth century three-terminal electronic device called a switch was invented. However the advancements in bipolar and field-effect semiconductor switching (which were invented in 1940-50’s) replaced the existing vacuum tube switches. Solid state switching circuits have revolutionized electronics tremendously since then; they play a key role as the fundamental components of modern computer systems. Basic semiconductor power switching devices include diodes (bipolar and Schottky), transistors (BJT and MOSFET), and thyristors [1] [2].

One of the major applications of a transistor is its usage in switching circuits in order to take advantage of its fast switching speed and substantial reliability at low cost over conventional mechanical relays by regulating current or voltage flow in a circuit. There has always been a growing need for transistors
which are faster, more rugged, and had higher current gain than their minority-carrier devices like BJT. As a result, switching power conversion became a commercial reality. Over the past few decades solid state switching has come a long way from current controlled switches such as bipolar junction transistors (BJT’s) to voltage controlled switches such as field effect transistors (FETs).

1.1.1 The BJT as a switch

We know that a transistor can be used as a switch simply by driving the device back and forth the cutoff and the saturation regions. The polarity of a BJT input is same as the polarity of its output wave, i.e., usage of a positive input signal produces a positive output signal. A basic BJT used as a switch along with its dc load line is shown in the Figure below.

![Figure 1-1: A BJT as a switch](image)

Figure 1-1: A BJT as a switch [3]
1.1.2 The JFET as a switch

Unlike a BJT, FET construction and operation is considerably different. In a FET, flow of current is controlled by an electric field. These FETs are classified broadly as follows:

- The junction field effect transistors (JFET)
- The metal-semiconductor Field effect transistors (MESFET)
- The metal-oxide semiconductor field effect transistors (MOSFET)
- The High electron mobility transistors (HEMT)

JFET and MESFET are quite similar in terms of construction and operation, only difference being JFET uses a PN junction for gate whereas MESFET uses a Schottky contact. A basic JFET as a switch is illustrated in the Figure below.

![Figure 1-2: A JFET as a switch [3]](image-url)
1.1.3 The MOSFET as a switch

The advantage of MOSFET being used as a switch is twofold: first, the dimension of the device is smaller compared to BJT thus increasing the component density; secondly, the manufacturing of these devices is easier and less expensive. Moreover this device has high input impedance at the same time the input-output voltages have same polarity, which are the leading features in JFET and BJT [3].

![Diagram of MOSFET as a switch]

**Figure 1-3: A MOSFET as a switch [3]**

1.2 Power MOSFETs

One of the main applications for FETs is its usage as solid state switches. However under normal circumstances FETs cannot be used for high power applications. Connecting several FETs in parallel may resolve this limitation and
may enable us to switch high current and voltage loads but doing so consumes a lot of board space which is impractical. To overcome these problems power switches/FETs were developed.

1.2.1 Silicon based power MOSFETs

For over 3 decades Silicon based FETs have been widely used for amplifying or switching electronic signals. These silicon based power transistors enabled high efficiency power conversion, a commercial reality. Unfortunately, silicon-based devices are reaching its performance limits of switching due to limitations of its processing speed, density, design complexity and heat dissipation. The major limitation of power devices is due to excessive amount of energy consumption, which is particularly the case in silicon based MOSFETs. These energy losses can be limited by reducing conduction losses due to resistance and also reducing switching losses during ON and OFF transition states, often there is a tradeoff between these two.

As energy losses incurred from existing silicon devices cannot be reduced due to this tradeoff, a search for materials began which had on-resistance(R) and threshold charge (Q) tradeoff greater than that of Silicon power MOSFET. This RQ product makes it crucial in determining the ‘Figure of merit’ of the silicon and gallium nitride based devices.
1.2.2  Gallium Nitride (GaN) and Silicon carbide (SiC) based power switches

A substantial amount of research was focused towards wideband gap materials such as GaN (band gap of 3.4 eV) and SiC (band gap of 3.23 eV) which had a potential to reduce the die size further and also improve the RQ product by more than a factor of 100 compared to Si (band gap of 1.12 eV) devices [4]. In spite the fact that both GaN and SiC offered several significant performance improvements such as higher power density, higher voltage, low leakage current and ability to operate at high temperatures, gallium nitride FETs were encouraged more than silicon carbide devices because of their higher efficiency and faster switching speed attained due to their material properties.

Although GaN based devices appeared to offer potential for much higher performance including higher operational frequency, they were not commercially encouraged initially due to drawbacks such as high device cost and device operating in depletion mode. However, the progress in the growth of the group III nitrides soon triggered advancement in the field GaN based High Electron Mobility Transistor (HEMT) technology. Initially, GaN HEMTs faced a lot of challenges in the power switches market, such as device operating in depletion mode, limited range of gate voltages and drain current collapsing at higher voltages, out of which many problems have been addressed with the help of years of research in the field of GaN. As part of this project, gallium nitride
power semiconductor devices are modelled and simulated by using Silvaco TCAD software for switching applications.

1.2.3 Introduction to GaN based High Electron Mobility Transistor (HEMT)

FETs like MOSFETs and HEMTs are preferred because they have a better thermal stability than a BJT. GaN based HEMT were first demonstrated in 1994 [5] but it was not until the year 2004, Eudyna corporation in Japan [6] manufactured the first ever depletion mode HEMT commercially.

![Figure 1-4: Formation of a 2DEG for an AlGaN/GaN hetero-structure](image)

In switching applications, depletion mode devices are inconvenient due to the need for applying a continuous negative bias until startup. To overcome this limitation after years of research EPC Corporation managed to manufacture first ever enhancement mode GaN based HEMT’s [7].

These HEMT’s are based on a hetero-junction device structure formed by joining of two different wide band gap materials such as AlGaN and GaN [8]. These nitride based transistors have demonstrated an unusually high electron mobility at the AlGaN/GaN interface, due to the strain induced polarization at
the interface which is commonly referred as the 2DEG (two dimensional electron gas) through which the conduction occurs in a HEMT.

The Figure 1-5, represents a plot depicting the observed band bending of the conduction band edge in HEMTs. It also illustrates the formation of quantum well below the fermi level at the AlGaN/GaN interface, which confines the electrons into a narrow space. Once the electrons are trapped in the well, electrons would then have motion in the quantized energy levels within the well.

Figure 1-5: Band diagram of a HEMT at the AlGaN/GaN interface [9]
Chapter 2  Modelling of Power Switches

2.1 Introduction

This chapter focuses on two main subjects. First, the underlying physics involved in methods and models is summarized. Second, a design modelling of various power switches using Silvaco TCAD (Technology computer-aided design) is presented. Design modelling includes investigation of breakdown voltages, voltage-current characteristics of various devices at varied temperatures, drain-source leakage currents and device circuit performance in order to assess the reliability of gallium nitride power devices.

In this thesis, we have used Silvaco TCAD device simulation tools (specifically Atlas module) to simulate the electrical and thermal behavior of gallium nitride based design models as close as possible to the commercially available gallium nitride power devices. We were unable to obtain the exact fabrication procedure and device design parameters from manufacturing companies as it is proprietary, so we tried to approximate those devices as close as possible by using published information in various research journals and publications.
2.2 Silvaco: TCAD simulation suite

Semiconductor simulation is broadly classified in two phases, viz. process simulation and device simulation. Since we do not have much access to fabrication details we limit the usage of process simulation models, however device simulation is extensively used to develop and optimize the semiconductor processes to design and predict the electrical characteristics of the device under test.

Other interactive tools such as Tony plot, Deck build, Tony plot 3D are also used in conjunction with the Silvaco Atlas. A device structure is simulated by defining the physical structure; it includes material specification, device models, numerical methods, etc. These models and method parameters help in solving the physical equations at specified bias conditions.

The device simulation stated in the input file should define the physical structure of the device, physical models that need to be considered, numerical methods that needs to be solved and electrical bias conditions at which it needs to simulate.

Of the available physical models in Atlas, recombination and generation, band gap narrowing, tunneling and temperature-dependent impact ionization are some of the most important models. A range of different mobility models with adjustable parameters are dependent on lattice temperature, impurity concentration, carrier concentration, carrier energy, parallel and perpendicular
electric fields. Transport models incorporate either Fermi–Dirac or Boltzmann statistics [10].

Atlas simulations execute the command and structure files to generate the corresponding output files which store the generated terminal voltages and currents obtained from the device analysis and also the solution files containing 2D and 3D solution data variables within the device at a given bias are stored and plotted using tools like Tony plot.

![Silvaco Atlas Flow chart](image)

Figure 2-1: Silvaco Atlas Flow chart [11]

### 2.3 Basic Semiconductor Equations

To understand and to depict the physical processes in the interior of a device, and to monitor the operation of modelled devices, it is vital to
understand the physical processes in semiconductor devices for credible prediction of their device characteristics.

This model consists of a set of fundamental equations, which link together the electrostatic potential and the carrier densities, equations like Poisson equation, transport equations and continuity equations for electrons and holes.

2.3.1 Poisson’s Equation

Poisson’s Equation relates the electrostatic potential to the space charge density:

$$\text{div}(\varepsilon \nabla \psi) = -\rho$$  \hspace{1cm} (1)

Where \(\psi\) is the electrostatic potential, \(\varepsilon\) is the local permittivity, and \(\rho\) is the local space charge density. The reference potential can be defined in various ways. The local space charge density is the sum of contributions from all mobile and fixed charges, including electrons, holes, and ionized impurities.

2.3.2 Transport Equations

The current density equations, or charge transport models, are usually obtained by applying approximations and simplifications to the Boltzmann Transport Equation. These assumptions can result in a number of different transport models such as the drift-diffusion model, the Energy Balance Transport Model or the hydrodynamic model. The choice of the charge transport model will then have a major influence on the choice of generation and recombination models which we decide to put in the physical models.
Additionally, transport equations are used in many drift diffusion models which in turn are used for wide applications in device simulations.

\[ J_n = -q\mu_n n \nabla \Phi_n \]  

(2)

\[ J_p = -q\mu_p p \nabla \Phi_p \]  

(3)

Where, \( q \) is the charge of the electron, while \( \mu_n \) and \( \mu_p \) represent the electron and hole mobility’s. \( \Phi_n \) and \( \Phi_p \) are the quasi-fermi levels.

2.3.3 Carrier Continuity Equations

The rate of change in carrier concentration for an infinitesimal region of material, is the difference between gradient of input-output flux and the total generation rate. The continuity equations for electrons and holes are defined by equations:

\[ \frac{\partial n}{\partial t} = \frac{1}{q} \text{div} J_n + G_n - R_n \]  

(4)

\[ \frac{\partial p}{\partial t} = \frac{1}{q} \text{div} J_p + G_p - R_p \]  

(5)

Where \( n \) and \( p \) are the electron and hole concentrations, \( J_n \) and \( J_p \) are the electron and hole current densities, \( G_n \) and \( G_p \) are the generation rates for electrons and holes, \( R_n \) and \( R_p \) are the recombination rates.
To perform process/device simulation programs in Silvaco, these model statements are highly essential and need to be used in the actual device simulation. The main concept that should be considered is to match the simulation methodology as close as possible to the fabrication technology in a manufacturing unit.

2.4 Defining a model structure in Atlas

For the past several years, there has been a lot of development activity aimed towards improving the device performance of wide band gap power devices. We are however more interested to model and simulate GaN power semiconductor devices using Silvaco TCAD Mixed Mode 2D Simulator for switching applications.

In order to understand how to build the structure and simulate a HEMT structure in Silvaco Atlas, we have undergone several steps to strengthen our basics on the test structures by starting to design simple semiconductor devices starting from diodes and moved on to MESFETS & MOSFETS before we can model an HEMT structure.

Device modelling in Silvaco is done using a text editor like Deckbuild. Atlas is a finite element method based software. In order to execute a list of commands for the simulation to compile, the input file should be properly crafted with a sequence of steps that includes mesh, region, electrode, doping, models and methods. Hence, the order in which statements occur in an Atlas
input file is important. There are five groups of statements that must occur in a particular order to avoid termination of the program. Figure 2-2 describes briefly the statements that need to be mentioned in the Silvaco Atlas simulation software.

![Table with Atlas command groups and statements](image)

**Figure 2-2: Atlas command groups with the primary statements [11]**

### 2.5 Device simulation Model for diodes and power FETs

In order to understand how to build the structure and simulate a HEMT structure in Silvaco Atlas, we have undergone several steps to strengthen our basics on the test structures by starting to design simple semiconductor devices
starting from diodes and moved on to MESFETS & MOSFETS before we can model an HEMT structure.

Our observation included noting the obtained I-V characteristics of the semiconductor devices at forward bias, reverse bias, characterizing them in enhancement and depletion mode etc., based on the devices selected and comparing them with existing examples, or reference textbooks.

2.5.1 Model for Silicon based P-N junction Diode

A diode is a two-terminal semiconductor device having a p–n junction that conducts current in only one direction [12], [13], [3]. To build a diode in Silvaco, we had to analyze the examples which could be accessed through Deckbuild. The Atlas manual gives you basics in order to get started.

The device structure specification is done by defining mesh regions in Atlas along x and y directions. Once the whole device region is defined using mesh statements, this defined physical structure is then loaded as input to Atlas, which is run in a DECKBUILD run-time environment to predict the electrical characteristics associated with specified bias conditions. Initially we have built a Silicon diode by joining a p-type and n-type material with a uniform doping concentration of $7.6 \times 10^{-13} \text{cm}^{-3}$ each.

In order to predict the electrical characteristics that are associated with the physical structure, we need to define material and model specification to provide approximation and interpolation. After defining a minimum set of material
definitions such as mobility of electrons and holes, recombination lifetimes of electrons and holes; physical models such as parallel electric field mobility, concentration mobility, Shockley Read Hall (SRH) Recombination, auger recombination and band gap narrowing models are included, which solve the semiconductor device problems. Method statements are used to solve the system of model equations.

All the material, model and method specifications define the physics involved in running the modeled semiconductor device. The solve statements are used for obtaining solutions; in this case DC solutions of the device are calculated. An initial first run is simulated by the ‘solve’ statement in which the anode bias is ramped up from 0V to 0.8V with 0.01V step increments to calculate the diode forward characteristic under room temperature conditions. A second Atlas run is performed to simulate the reverse and breakdown characteristics of the device under room temperature conditions. The obtained I-V data is saved in the log file and displayed using Tony-plot.

Using ATLAS, we specify device simulation problems by defining:

- The physical structure to be simulated.
- The physical models to be used.
- The bias conditions for which electrical characteristics are to be simulated.
By the end of the P-N diode simulation we were able to design a device structure with 200 X 15 micron dimensions with $7.6 \times 10^{-13}$ cm$^3$ doping concentration of p-type and n-type silicon. Below is an illustration of the designed P-N diode in Silvaco Atlas device structure.
Figure 2-4: Forward bias characteristics of a P-N power diode

Figure 2-5: Reverse bias characteristics of a P-N power diode until breakdown.
The obtained output graphs show the forward and reverse bias electrical characteristics for a power diode at room temperature using Tony-plot. The obtained I-V plots are measured in Amps and Volts. From Figures 2-5 and 2-6 it is inferred that the barrier potential of the diode is 0.65 V and the breakdown voltage of the diode in reverse bias is 1550 V.

2.5.2 Model for Silicon Carbide Based Schottky Diode

Upon successful modeling of the P-N diode, we moved on to build a Schottky diode. A basic Schottky diode is a diode with a low forward voltage drop and a very fast switching action. Its device structure is similar to an ordinary bipolar P-N diode but with a metal-semiconductor junction (Schottky contact) at the anode terminal. We have chosen to design a Schottky diode due to its metal-semiconductor junction, as it would be very useful for modeling contact terminals for advanced high speed devices such as MESFETs and HEMT’s [12], [13].

We have modeled the Schottky diode with heavily doped uniform n-type Silicon material ($1.0 \times 10^{-20} \text{ cm}^{-3}$) below a Gaussian doped ($1.0 \times 10^{-15} \text{ cm}^{-3}$) floating n-type Silicon region. The Schottky anode is located at the top of the device, while the cathode terminal is located at the bottom of the device. The
syntax statement for setting a Schottky contact is “contact name=<char> work function=<val>”. It is used to specify the work-function of the Schottky electrode.

After specifying material, model and method specifications in the 200 x 20 micron Schottky diode the anode is ramped up from 0 to 1V in 0.01V steps to measure the forward bias simulation. A second Atlas run is performed to simulate the reverse and breakdown characteristics, it is done by ramping up the cathode voltage from 0V to 32V with various step sizes under room temperature conditions. The obtained I-V data is saved in the log file and displayed using Tony-plot.

![Figure 2-6: Schottky diode device structure.](image)
Figure 2-6 represents a plot for the Schottky diode. Due to metal semiconductor junction along with a Gaussian doping profile, the depletion width is towards semiconductor region.

Figure 2-7: Forward bias characteristics of a Schottky diode.
The obtained output graphs show the forward and reverse bias electrical characteristics for a Schottky diode at room temperature using Tony-plot. The obtained I-V plots are measured in Amps and Volts.

From the Figures 2-7 and 2-8 it is clear that the barrier potential of the Schottky diode is 0.62 V and the soft breakdown occurs at 45 Volts under reverse bias conditions.

Upon comparing the I-V characteristics of the SiC Schottky diode along with P-N diode it is evident that both the devices have a similar voltage drop but Schottky diode has a lower breakdown voltage.
2.5.3 Model for Gallium Arsenide based MESFET

Next, we moved on to modeling of transistors. We had to undergo several challenges when we first moved on to simulate a MESFET.

MESFET is an acronym for metal–semiconductor field effect transistor. The metal–semiconductor formed is a Schottky contact [12], [14]. The previous modeling of Schottky diode gave us in depth knowledge how to model the metal–semiconductor junction of the MESFET.

MESFET modelling is similar to a JFET provided it would use a Schottky contact as there gate terminal while source and drain terminals are ohmic contacts. The solution sequence for MESFET threshold voltage, is first to obtain the initial solution at zero bias on all contacts. By knowing the threshold voltage we can model MESFET in enhancement mode or depletion mode. A GaAs MESFET is modelled using Silvaco in both of these modes of operation.
A 0.12 micron layer thickness of heavily doped N+ GaAs ($1.0 \times 10^{-17}$ cm$^3$) is sandwiched with a moderately doped ($1.0 \times 10^{-15}$ cm$^3$) p-type GaAs for an enhancement mode device operation. The corresponding device structure in Silvaco is illustrated in Figure 2-9.

A depletion mode operation of MESFET with the doping concentration of an 0.12 micron layer thick N+ GaAs is further heavily doped ($1.3 \times 10^{-17}$ cm$^3$) and deposited over the moderately doped ($1.0 \times 10^{-15}$ cm$^3$) p-type GaAs substrate layer using Silvaco as shown in Figure 2-11.
Figure 2-10: MESFET enhancement mode I-V characteristics

Figure 2-11: MESFET Depletion mode I-V characteristics
The obtained plots 2-10 and 2-11 show the enhancement and depletion mode operation of MESFET at room temperature using Tony-plot. The obtained I-V characteristics are measured in Amps and Volts. It is observed that the current does not reach saturation at higher drain voltages.

2.5.4 Model for silicon based MOSFET

It is an acronym for Metal Oxide Semiconductor Field Effect Transistor. The structure of the MOSFET is similar to that of a MESFET; there is an additional oxide layer present in between metal and the semiconductor layer [12], [13], [3]. An oxide layer induces a conducting channel between source and drain terminals with the application of small applied bias voltages to the gate terminal. In our case we modelled a Si based MOSFET having an n-type Gaussian doping profile (1.0 x 10^{-16} cm^{-3}) under the source and drain terminals. Additionally the device structure has a gate metal contact under which is an oxide layer with thickness of 20 nm, while the source and drain are left as ohmic contacts.
Figure 2-12: MOSFET device structure using Silvaco showing Gaussian doping concentrations.

In an enhancement mode MOSFET, a drain current will only flow when a gate voltage ($V_{GS}$) greater than the threshold voltage ($V_{TH}$) is applied to the gate terminal. This device's breakdown performance is also illustrated in the Figure below.
Figure 2-13: MOSFET enhancement mode I-V characteristics with breakdown.

The obtained output graphs show the forward characteristics of a MOSFET along with its breakdown voltage at room temperature using Tony-plot. The obtained I-V plots are measured in Amps and Volts. It is observed that the breakdown voltage of this FET is quite low.
Chapter 3  Gallium Nitride (GaN) Power FETs

3.1 Introduction to HEMTs

The need for power devices having high power and high efficiency has never been more important in the recent years. With silicon based switching devices closing in towards their theoretical limits of performance, GaN HEMT stood out to be the emerging technology that could replace silicon power devices. GaN FETs have unlocked new applications in the semiconductor industry because of their ability to switch high voltages and high currents at faster transients than any transistor before. With major advances in the field of wide band gap semiconductor devices and growth of the group-III nitrides, have led to the development of AlGaN/GaN high electron mobility transistors (HEMTs). The related applications offer great potential for GaN including, such requiring high critical electric field which would enable GaN to withstand much greater voltage [4].

When we compare the properties of different materials, GaN-based HEMTs have many advantages over other technologies (e.g., GaAs). For instance the high output power density of GaN allows the fabrication of much smaller
size devices compared to GaAs with the same output power. According to maximum power transfer theorem, matching load and source impedances with each other will achieve maximum power [15]. Having high impedance for a small sized device allows reducing power losses that are due to load matching in amplifiers [15] (e.g., ten times larger load matching might be needed for a GaAs transistor, increasing overall complexity and cost). The operation at high voltage due to its high breakdown electric field not only reduces the need for voltage conversion, but also provides the potential to obtain higher efficiency, which is a critical parameter for amplifiers [16]. The wide band gap also enables it to operate at high temperatures. At the same time, the HEMT offers better noise performance than that of MESFETs [17].

Table 1: Material properties for various semiconductors at high frequencies

<table>
<thead>
<tr>
<th>Material</th>
<th>Si</th>
<th>GaAs</th>
<th>4H-SiC</th>
<th>GaN</th>
<th>Diamond</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_g$ (eV)</td>
<td>1.1</td>
<td>1.42</td>
<td>3.26</td>
<td>3.39</td>
<td>5.45</td>
</tr>
<tr>
<td>$n_i$ (cm$^{-3}$)</td>
<td>1.5x10$^6$</td>
<td>1.5x10$^6$</td>
<td>8.2x10$^{-9}$</td>
<td>1.9x10$^{-10}$</td>
<td>1.6x10$^{-27}$</td>
</tr>
<tr>
<td>$\epsilon_r$</td>
<td>11.8</td>
<td>13.1</td>
<td>9.0</td>
<td>1.0</td>
<td>5.5</td>
</tr>
<tr>
<td>$\mu_n$ (cm$^2$/V s)</td>
<td>1350</td>
<td>8500</td>
<td>700</td>
<td>1200(Bulk)</td>
<td>1900</td>
</tr>
<tr>
<td>$v_{sat}$ (10$^7$/cm/s)</td>
<td>1.0</td>
<td>1.0</td>
<td>2.0</td>
<td>2.5</td>
<td>2.7</td>
</tr>
<tr>
<td>$E_{br}$ (MV/cm)</td>
<td>0.3</td>
<td>0.4</td>
<td>3.0</td>
<td>3.3</td>
<td>5.6</td>
</tr>
<tr>
<td>$\Theta$ (W/cm K)</td>
<td>1.5</td>
<td>0.43</td>
<td>3.3-4.5</td>
<td>1.3</td>
<td>20</td>
</tr>
<tr>
<td>$J_M = \frac{E_{br}v_{sat}}{2\pi}$</td>
<td>1</td>
<td>2.7</td>
<td>20</td>
<td>27.5</td>
<td>50</td>
</tr>
</tbody>
</table>

A HEMT device structure is formed by joining two or more different band gap materials. Due to the formation of a hetero-structure junction a “pool” of two-dimensional electron gas (2DEG) is induced at its junction and is enhanced
by the polarization strain, which is intrinsic in GaN-based hetero-structures [18]. This newly formed pool of electrons is through which the conduction occurs in a HEMT [19]. Gallium nitride cannot be grown directly over a silicon substrate due to lattice mismatch between the materials, at the same time having a GaN substrate is also not realizable due to limited availability of the bulk GaN. In general, to reduce the cost of manufacturing GaN HEMTs are grown over a silicon substrate by placing a buffer layer such as AlN in between, to avoid excessive strain on the lattice structure.

The most important point about the channel layer in the HEMT devices is the 2DEG that results from the band-gap difference between Al$_x$Ga$_{1-x}$As/GaAs or Al$_x$Ga$_{1-x}$N/GaN. Illustrated in Figure 3-1 is the band diagram of a generic HEMT showing the 2DEG formed due to different band gaps.

The 2DEG is formed since the higher band gap of Al$_x$Ga$_{1-x}$N allows free electrons to diffuse from the Al$_x$Ga$_{1-x}$N to the lower band gap GaN near the interface. A potential barrier then confines the electrons to a thin sheet of charge known as the 2DEG.

In contrast to the MESFET, which has a doped channel and consequently lots of ionized donors, the 2DEG has significantly less Coulomb scattering, resulting in a very high mobility device structure. The remainder of the HEMT structure contains an Al$_x$Ga$_{1-x}$N spacer layer, a donor layer n+ Al$_x$Ga$_{1-x}$N, an n Al$_x$Ga$_{1-x}$N Schottky contact layer, and a highly doped n+ GaN layer. The spacer
layer serves to separate the 2DEG from any ionized donors generated by the pulse doping or n+ active layer. The drawback of the spacer layer, however, is that the sheet carrier concentration (total amount of charge) in the channel is reduced as the spacer layer thickness is increased [20].

Figure 3-1: Energy band diagram of a generic AlGaN–GaN HEMT showing the 2DEG quantum well channel.

3.2 Polarization charges in an AlGaN/GaN HEMT

Both AlGaN and GaN have polarized Wurtzite (hexagonal) crystal structures, in which electric dipoles are arranged in the [0001] direction across the crystal as shown in Fig. 3-2. At zero bias, this macroscopic polarization includes spontaneous (pyro-electric) and strain induced (piezo-electric) contributions [21], [22], [23], [24]. The primary effect of polarization is due to accumulation of charge at the AlGaN/GaN hetero interface caused by the abrupt divergence in the polarization.
Figure 3-2: AlGaN/GaN Crystal structures and there polarization effects [24]

Usually polarization vector in a GaN crystal contains only the spontaneous component, \( P_{SP} \) (GaN). But for AlGaN layer, in addition to the spontaneous component \( P_{SP} \) (AlGaN), a piezo-electric polarization component \( P_{PE} \) (AlGaN) is also present. This additional piezo electric polarization component is due to the presence of strain in the \( Al_xGa_{1-x}N \) alloy when aluminum is added to GaN.

Spontaneous polarization at the AlGaN/GaN interface is calculated by

\[
P_{SP} (AlGaN/GaN) = P_{SP} (Al_xGa_{1-x}N) - P_{SP} (GaN) = \text{constant, depends on } x \tag{6}\]

Piezo-electric polarization component in AlGaN layer is given by

\[
P_{PE} (AlGaN) = 2\varepsilon [e_{31} - e_{33} (c_{33})] \tag{7}\]

The aluminum content present in AlGaN alloy causes piezoelectric strain.
3.3 A Basic GaN Transistor Structure

Just like all other FETs there are two modes of operation in a HEMT viz., depletion mode and enhancement mode. A basic depletion mode (normally ON) GaN HEMT is shown in the Figure 3-4 below. Upon applying a negative bias to the gate terminal, the electrons in the 2DEG are depleted, this reduction of electrons controls the flow of current in the device.

![Figure 3-3: A basic Depletion mode HEMT with negative bias](image)

For high voltage power switching applications, gallium nitride-based power transistors need to operate in *Normally OFF operation (enhancement mode)*. We would discuss various cases of normally OFF operated HEMT devices.

Some of the structures used in enhancement mode HEMT devices are

1. Schottky gate [18], [25]
2. Recessed gate [26], [27], [28]
3. Fluorine plasma ion implant gate [29]
4. P-GaN gate [30], [31]
A basic enhancement mode (normally OFF) GaN HEMT is shown in the Figure 3-4 below. Upon applying a positive potential to the gate terminal, a 2DEG is formed under the gate terminal which would then complete the circuit, allowing current to flow between the drain and the source terminals.

Figure 3-4: A basic enhancement mode HEMT with positive bias

When building an AlGaN/GaN transistor either to operate in depletion mode or enhancement mode, most of the fabrication steps involved are similar such as selection of substrate material, growing of the AlN as a seed layer, deposition of GaN layer followed by AlGaN layer to create strain in the device. Light doping of the AlGaN layer and forming electrical contacts etc. Apart from this simplified process, based on the specific device structure additional process steps are performed as required.
Chapter 4  Results and Discussions

4.1  I-V characteristics

4.1.1  Depletion mode

Initial development of a generic test structure is done for HEMT using Silvaco. We have referred various journal papers to model depletion mode GaN based HEMT structures. Initially, we have simulated the cross sectional view discussed by Sona P.Kumar et al. [32], in Silvaco Atlas based on the specifications given in the journal paper and assuming the other unknown quantities. The charge control model consists of a hetero-junction of AlGaN and GaN, the hetero-interface of the wide band gap AlGaN and narrow band gap GaN layers form a two-dimensional electron gas (2DEG) which is the main reason for the high mobility of electrons in this structure. The current-voltage characteristic output results obtained after replicating the journal paper device structure in Silvaco Atlas are compared with one another.
The structure of the depletion mode device is illustrated in Figure 4-1 below; where \( L \) denotes the device gate length, \( d_d \) denotes the thickness of the n-AlGaN layer and \( d_s \) is the spacer layer thickness.

![Cross-sectional view of AlGaN/GaN MODFET](image)

**Figure 4-1:** Cross sectional view of AlGaN/GaN MODFET [32].

Based on the above model structure we have realized the following characteristics of the device model from the journal paper [32].

**Table 2:** Material properties of a depletion mode HEMT

<table>
<thead>
<tr>
<th>Material Properties</th>
<th>Device values</th>
</tr>
</thead>
<tbody>
<tr>
<td>AlGaN doping (n doped)</td>
<td>2 X 10^{-18} cm(^{-3}) (Moderately doped)</td>
</tr>
<tr>
<td>GaN doping (n doped)</td>
<td>1 X 10^{-15} cm(^{-3}) (Lightly doped)</td>
</tr>
<tr>
<td>Aluminum composition in AlGaN</td>
<td>15%</td>
</tr>
<tr>
<td>Parameter</td>
<td>Value</td>
</tr>
<tr>
<td>-------------------------------</td>
<td>-------------</td>
</tr>
<tr>
<td>GaN mobility</td>
<td>1370 cm²/v-s</td>
</tr>
<tr>
<td>Saturation velocity</td>
<td>2.1 X 10⁷ cm/s</td>
</tr>
<tr>
<td>Gate contact</td>
<td>Schottky</td>
</tr>
<tr>
<td>dₙ (thickness of the n-AlGaN)</td>
<td>36 nm</td>
</tr>
<tr>
<td>dᵢ (spacer layer thickness)</td>
<td>4 nm</td>
</tr>
</tbody>
</table>

The layer structure obtained by simulating the device in Silvaco with the above specifications is shown in Figure 4-2.

**Figure 4-2: HEMT depletion mode device structure modeled in Silvaco Atlas.**

Finally, to analyze the behavior of the simulated device it is now compared with the AlGaN/GaN device I-V characteristics shown in the paper.
Figure 4-3 shows the I-V characterization resemblance. Note that the modelled device is a 2D model with its default width (in Z - direction) set to be 1 μm. On the other hand, the model discussed in the journal has a width of 1mm. To extrapolate and match the results of the simulation, die size needs to be matched that is why it is essential to multiply the output drain current to the order of 1000, to be able to compare the results.

Figure 4-3: I-V Characteristics provided by the journal paper [32] (left) and Silvaco modelled device (right) are compared

Upon comparison, it is evident that the results of the model are in a good agreement with the journal’s data with slight discrepancy. However at higher voltages significant gate leakage and substrate current are observed in the graph of my simulated device without further increasing the gate potential which is an
undesirable effect. Our project required us to focus more towards enhancement mode devices as they are more suited for power applications.

4.1.2 Enhancement mode

The enhancement mode AlGaN/GaN HEMTs would greatly enhance the application potential of GaN devices by limiting the power dissipation which is widely observed in depletion mode devices. As part of our project, in order to compare the device performance of simulated and measured GaN based power switches, it is crucial to simulate enhancement mode devices as they are extensively reliable for high voltage power switching applications. Earlier we have discussed various types of enhancement mode device operations; we shall model each of those types.

4.1.2.1 Schottky gate enhancement mode structure

The following is a GaN based HEMT, which is carefully design engineered to incorporate an Schottky gate contact to obtain key desirable features like normally OFF operation, high breakdown voltage, reduced current collapse and high drain current.

Schottky gate contacts are one of the most extensively used methods for manufacturing of HEMT structures. They deplete the 2DEG formed beneath the gate terminal but once a positive voltage is applied to the gate, the 2DEG path is reestablished and device switches to conduction.
Based upon the journal papers [18], [25] and other published papers from Silvaco [33], several parameters that are approximated from these references are used to model the Schottky gate enhancement mode structure. The device specifications used for this simulation to achieve enhancement mode operation, high breakdown voltage etc. are as follows:

Table 3: Material properties of a Schottky gate HEMT

<table>
<thead>
<tr>
<th>Material Properties</th>
<th>Device values</th>
</tr>
</thead>
<tbody>
<tr>
<td>AlGaN doping (n doped)</td>
<td>$3.7 \times 10^{-17}$ cm$^{-3}$ (Moderately doped)</td>
</tr>
<tr>
<td>GaN doping (n doped)</td>
<td>$3.7 \times 10^{-13}$ cm$^{-3}$ (Lightly doped)</td>
</tr>
<tr>
<td>Aluminum composition in AlGaN</td>
<td>20%</td>
</tr>
<tr>
<td>GaN mobility</td>
<td>1370 cm$^2$/v-s</td>
</tr>
<tr>
<td>Thickness of AlGaN layer</td>
<td>10 nm</td>
</tr>
<tr>
<td>Thickness of GaN layer</td>
<td>300 nm</td>
</tr>
<tr>
<td>Gate contact</td>
<td>Schottky</td>
</tr>
<tr>
<td>Work function of Schottky gate</td>
<td>6.3 eV</td>
</tr>
</tbody>
</table>

Fig. 4-4 represents the 2D modelled device structure with a Schottky gate.
Figure 4-4: Enhancement mode (Normally OFF) HEMT device structure modeled in Silvaco Atlas

Figure 4-5: Electron concentration for a Schottky HEMT (zoomed at the interface)
Figure 4-5 illustrates the depletion of the electrons in the 2DEG underneath the gate terminal at zero bias for a normally OFF device.

![Band diagrams of the enhancement mode HEMT device structure](image)

**Figure 4-6:** Band diagrams of the enhancement mode HEMT device structure; underneath the gate terminal (center) and in midst of gate-drain (right)

Energy band diagrams shown in Figure 4-6 show that the quantum wells are formed in a HEMT along the hetero-junction, except under the gate terminal. These quantum wells are formed due to the difference in the band gap of AlGaN and GaN layers. However, the presence of higher gate work-function leads to contraction of the quantum well below the gate contact. Also, the field depends on applied gate bias.
The structure of the 3-dimensional Schottky HEMT is demonstrated in Figure 4-7.

![3D plot of a 3D enhancement mode HEMT device structure](image)

Figure 4-7: 3D plot of a 3D enhancement mode HEMT device structure

Physical device models such as spontaneous and piezoelectric polarization is specified in the region statements to calculate strain induced due to lattice mismatch. Additionally physical models like parallel electric field mobility, concentration dependent mobility [34], Shockley Read Hall (SRH) Recombination [35], Auger recombination [36] and band gap narrowing models [37] etc. are also included in the device simulation to replicate velocity saturation effect, temperature dependence, carrier lifetimes and recombination lifetimes of majority and minority carriers at high current densities. These mathematical
models better describe semiconductor device physics, which are essential to plot the I-V characteristics.

![HEMT enhancement mode device structure](image)

**Figure 4-8:** Schottky HEMT enhancement mode (Normally OFF) I-V Characteristics.

The realized I-V characteristics are plotted while gate voltages is varied from 0V to 5V. The simulated results show the effect of gate voltage upon the drain current, which is flowing in between the source and drain terminals. It is observed that the ON resistance of a Schottky HEMT is decreased when compared to ohmic HEMT devices.
4.1.2.2 Recessed gate enhancement mode structure

As the name of the structure suggests, it utilizes a Schottky contact which is fabricated by recessing the gate terminal into the AlGaN layer, in order to reduce the voltage generated by piezoelectric field. When the built-in work function of the metal contact is higher than the strain voltage, it breaks the 2DEG underneath the gate terminal unless an additional voltage is applied to recombine the 2DEG. The modelled recessed gate HEMT structure was based on the literature [38] with few additions to the design structure to achieve higher current gain. The following specifications of the device model are considered

<table>
<thead>
<tr>
<th>Material Properties</th>
<th>Device values</th>
</tr>
</thead>
<tbody>
<tr>
<td>AlGaN doping (n doped)</td>
<td>$3.7 \times 10^{-17} \text{ cm}^{-3}$ (Moderately doped)</td>
</tr>
<tr>
<td>GaN doping (n doped)</td>
<td>$3.7 \times 10^{-13} \text{ cm}^{-3}$ (Lightly doped)</td>
</tr>
<tr>
<td>Aluminum composition in AlGaN</td>
<td>20%</td>
</tr>
<tr>
<td>GaN mobility</td>
<td>1370 cm$^2$/v-s</td>
</tr>
<tr>
<td>Thickness of AlGaN layer</td>
<td>10 nm</td>
</tr>
<tr>
<td>Thickness of GaN layer</td>
<td>600 nm</td>
</tr>
<tr>
<td>Gate contact</td>
<td>Schottky</td>
</tr>
<tr>
<td>Work function of Schottky gate</td>
<td>6.3 eV</td>
</tr>
</tbody>
</table>
Figure 4-9: Recessed gate enhancement mode (Normally OFF) HEMT device structure modeled in Silvaco Atlas

Figure 4-10: Electron concentration in an enhancement mode Recessed gate HEMT (zoomed at the interface)
Recessed gate structure along with the amount of electron concentration flowing through the device is illustrated in Figures 4-9 and 4-10.

The measured I-V characteristics clearly show the normally off operation of the device measured at room temperature 25°C having desired features like normally OFF operation, high breakdown voltage, reduced current collapse and high drain current. It is in a good agreement with the rated performance of a HEMT structure.

Physical device models such as spontaneous and piezoelectric polarization are specified in the region statements to calculate strain induced due to lattice mismatch. Additionally, physical models like parallel electric field mobility, concentration dependent mobility [34], Shockley Read Hall (SRH) Recombination [35], Auger recombination [36] and band gap narrowing models [37] etc. are also included in the device simulation to replicate velocity saturation effect, temperature dependence, carrier lifetimes and recombination lifetimes of majority and minority carriers at high current densities. These mathematical models better describe semiconductor device physics, which are essential to plot the I-V characteristics.

The plot represents the dc characteristics at lower voltages, but it has been observed that the current collapse is larger in recessed gate HEMTs compared to conventional HEMTs.
Figure 4-11: Recessed gate HEMT enhancement mode (Normally OFF) I-V Characteristics.

The simulated results show the effect of gate voltage upon the drain current, which is flowing in between the source and drain terminals. The dc characteristics of a normally OFF device are plotted while gate voltages is varied from 0V to 5V. From Figure 4-11 it is evident that the ON resistance of a recessed HEMT has been improved when compared to Schottky HEMT devices. Upon using the recessed gate, the performance of GaN transistors is improved by achieving high breakdown voltage and high threshold voltage.
4.1.2.3 P-GaN gate enhancement mode structure

Extensive manufacturing of a recessed gate HEMT is a tedious task due to its complex design structure, and more over precise etching of AlGaN layer is not realizable on a large scale production environment. Another popular device structure which is used to create enhancement mode devices is using a P-GaN gate device structure. The device structure of P-GaN gate is easier to manufacture compared to recessed gate due to its simple design.

A TCAD device simulation is performed to model a P-GaN gate HEMT. Its design is slightly different from the other enhancement mode structures; it utilizes a P doped GaN layer under the ohmic metal gate contact which helps in reducing the piezoelectric effect in the device. Also, the AlGaN and GaN layers are un-doped. The following specifications of the device model are considered to simulate P doped GaN device.

Table 5: Material properties of a P-GaN HEMT

<table>
<thead>
<tr>
<th>Material Properties</th>
<th>Device values</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN doping</td>
<td>Un-doped</td>
</tr>
<tr>
<td>AlGaN doping</td>
<td>Un-doped</td>
</tr>
<tr>
<td>P-GaN gate doping</td>
<td>$3 \times 10^{-17}$ cm$^{-3}$</td>
</tr>
<tr>
<td>Aluminum composition in AlGaN</td>
<td>23% (Cap layer)</td>
</tr>
<tr>
<td>Aluminum composition in AlGaN</td>
<td>5% (Transition layer)</td>
</tr>
</tbody>
</table>
### GaN mobility
1370 cm²/v-s

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thickness of AlGaN layer</td>
<td>15 nm</td>
</tr>
<tr>
<td>Thickness of GaN layer</td>
<td>50 nm</td>
</tr>
<tr>
<td>Thickness of substrate</td>
<td>2 µm</td>
</tr>
<tr>
<td>Gate contact</td>
<td>P-GaN (Ohmic)</td>
</tr>
</tbody>
</table>

Figure 4-12: P-GaN gate Enhancement mode (Normally OFF) HEMT device structure modeled in Silvaco Atlas

One major challenge which we came across while modelling P-GaN gate Enhancement-Mode Structure is its current collapse, we did some literature survey regarding the same and found that both passivation of the surface of
AlGaN layer and usage of field plates are known to mitigate the current collapse in gallium nitride based HEMT [39], [40], [41], [42], [43].

Based on the journal papers discussions we have modelled the device specification for the P-GaN HEMT structure. The electron concentration modelled using Silvaco for the P-GaN gate is shown in Figure below.

For the modelled P-GaN gate enhancement mode HEMT device structure, initially observed a significant amount of current collapse due to internal lattice heating. Initially we did not observe a lot of difference, but now when we look
more closely, there is a slight reduction in current collapse using gate field plate and dual field plate (gate field plate and source field plate) unfortunately a complete reduction of current collapse is not observed. Furthermore, to avoid excessive current collapse, the device model is implemented with low field mobility of electrons. To have a more realistic design, high density of donor traps (1 X 10^{21} \text{ cm}^{-3}) are introduced under the gate terminal in Figure 4-14.

![Figure 4-14: P-GaN gate HEMT Enhancement mode (Normally OFF) I-V Characteristics.](image)

The simulated results show the effect of gate voltage upon the drain current, which is flowing in between the source and drain terminals. The dc characteristics of a normally OFF device are plotted while gate voltages is varied
from 0V to 5V. From Figure 4-14 it is evident that the ON resistance of a recessed HEMT is better than that of ohmic HEMT devices.

The performance of P-GaN gate is similar to recessed gate HEMT, high breakdown voltage and high threshold voltage. There is a high amount of current collapse present in GaN transistors at higher gate voltages, this effect can be mitigated by use of field plates [43]. Manufacturing of P-GaN HEMTs on a large scale is more feasible compared to recessed gate HEMTs, and also the current collapse is larger in recessed gate HEMTs compared to conventional HEMTs thus P-GaN HEMTs are more encouraged.

4.2 High Temperature Reverse Bias Leakage Current

Power semiconductor devices which use wide band gap semiconductor materials such as gallium nitride (GaN), need to withstand high voltages and temperatures. To test the reliability of GaN based power devices, the drain-source voltage ($V_{DS}$) is ramped keeping the gate-source voltage zero. This test allows measuring the leakage current present in the device. To study the failure mechanism of the power devices, the leakage current is measured as a function of temperature.

The GaN based enhancement mode device is simulated under different temperatures ranging from 300 K to 500 K, to measure the drain-source leakage currents.
Figure 4-15: Modelled drain-source leakage for varying temperatures

A plot of current vs voltage is shown in Figure 4-15 with the temperature as a parameter. A GaN device (EPC 2012) was tested on a printed circuit board with its gate shorted to source by my research partner [44]. The temperature was ramped up from 0ºC to 200 ºC (300K to 500K) by placing the DUT on a chuck, which could control the temperature in a precise manner.
Figure 4-16, represents a semi-log plot of I-V characteristics, the rectangular box in the plot represents the simulated range shown in figure 4-15.

Upon comparison of the semi-log plots shown above in Figures 4-15 and 4-16, a similar leakage current is observed for the simulated and experimentally calculated results at high temperatures (500K).

In another scenario, GaN based enhancement mode device is simulated under different temperatures ranging from 300 K to 500 K, with the drain-source voltage \( V_{DS} \) set to be 15V which is the rated maximum for this device, to measure the temperature ramping effect on leakage current.
Figure 4-17: Temperature ramping effect on leakage current

The plot demonstrates the exponential temperature dependence of the simulated GaN device with respect to its leakage current. This particular simulation combines the electrical and thermal stress, which can help us to better understand the GaN device properties and its degradation effects. It is important to note that the voltage and temperature are monitored in such a way that the device doesn’t breakdown.

4.3 Circuit Simulation Model of GaN HEMT

To compare the switching operation of modelled GaN HEMT with commercially available EPC 2012, a simple circuit model is first designed and
simulated in PSPICE circuit simulator. The switching element described in PSPICE, its net list has been imported from device manufacturer’s website.

Later, the same circuit is realized in SILVACO MixedMode® with the previously modelled GaN based enhancement mode HEMT device structure discussed earlier as the switching element, the obtained results from both the simulations are compared.

4.3.1 Circuit 1: GaN device along with a resistor

The circuit shown in Figure 4-18 evaluates the switching behavior of a commercially available GaN power HEMT [45] along with a resistor using PSpice.

![Diagram of Circuit 1: GaN device along with a resistor](image)

Figure 4-18: Switching operation in a normally–off EPC 2012/GaN device.

The modelled circuit consists of a pulse generator which toggles the DUT ON and OFF every 10 nsec, while a constant 20 V DC power supply is being applied to the V_Ds.
In Figure 4-19, a transient response is plotted to assess the switching response of the DUT in PSpice. Upon applying a gate pulse as input (red wave) to the circuit, the FET acting as a switch is closed allowing current to flow through least resistance path. Corresponding voltage, $V_{DS}$ (blue wave) and current, $I_{DS}$ (green wave) switching behavior is represented.

To compare the device response, the same circuit is kept alongside the circuit description of PSPICE and is modelled in Mixed-Mode simulator using the previously designed enhancement mode device structure as the DUT. Note that, Mixed-Mode is a Circuit simulator in SILVACO which has the capability to simulate physics based devices such as GaN based power devices.
Figure 4-20: Simulation results obtained for circuit 1 using Mixed-Mode circuit simulator

The corresponding output presented from Mixed-Mode circuit simulator shows that upon applying a gate pulse (red wave), the physically based HEMT immediately switches ON without much lag in the switching voltage $V_{DS}$ (blue wave). Upon comparison, the results show that the realized physically based GaN HEMT device that the voltage ($V_{DS}$) and drain current ($I_{DS}$) switches very fast in the case of realized physically based GaN HEMTs but it’s not the same case in an actual device (EPC 2012). However, similar voltage spike is observed during drain current switching.
4.3.2 Circuit 2: GaN device along with an ideal diode

In the circuit shown in Figure 4-21, a GaN FET and ideal diode (Junction Capacitance=1pF and Transit time=100ps) are utilized to represent a circuit similar to half bridge to switch ON and OFF complimentary to each other. Half bridge is one of the most widely used switching topologies used for power electronic applications.

Figure 4-22: Simulation results obtained for Circuit 2 using PSPICE circuit simulator
In Figure 4-22, a transient response is plotted to assess the switching response of the DUT in PSpice. Upon applying a gate pulse as input (red wave) to the circuit, the FET acting as a switch is closed allowing current to flow through least resistance path. Corresponding voltage, $V_{DS}$ (blue wave) and current, $I_{DS}$ (green wave) switching behavior is represented.

The switching response of the modelled device is compared with the obtained simulation results using Silvaco.

Figure 4-23: Simulation results obtained for circuit 2 using Mixed-Mode circuit simulator
Upon comparison, the results show that the realized physically based GaN HEMT device and the actual device (EPC 2012) observe the spike during DUT switching.

4.3.3 Measured device results and simulated device results

The following Figure 4-27, is the schematic of the test circuit (EPC9010) that was used to measure the switching behavior of the half bridge circuit. The GaN FETs are given a complimentary input using a gate driver while a bypass capacitor is included to help smooth out the ripples in the power supply.

![Block diagram of EPC9010 Development Board](http://epc-co.com/epc/Portals/0/epc/documents/spice-files/PSPICE/EPC2012_V102_PSPICE.net)

To compare the switching performance of commercially available EPC device with the modelled device, a simplified version of Figure 4-24 is simulated using PSpice (the netlist can be found at [http://epc-co.com/epc/Portals/0/epc/documents/spice-files/PSPICE/EPC2012_V102_PSPICE.net](http://epc-co.com/epc/Portals/0/epc/documents/spice-files/PSPICE/EPC2012_V102_PSPICE.net)) and Silvaco MixedMode as shown in Figure 4-25.
The circuit uses two e-GaN FETs, which switch ON and OFF complementary to each other. The switching behavior (of the upper e-GaN FET) is shown below in Figure 4-26.
In the Figure 4-26, e-GaN FET switching behavior is observed at 1MHz frequency. The drain terminal of the DUT (orange waveform) is biased with a constant power supply of 40V. Upon DUT turn ON, a sudden drop of the voltage is observed at the source terminal (green waveform). The actual switching behavior can be observed by subtracting the drain voltage with respect to source voltage ($V_{DS}=V_D-V_S$), it is represented by pink waveform.

Figure 4-27: Simulation results obtained for Circuit 3 using PSPICE circuit simulator
The switching behavior (of the upper e-GaN FET as DUT) is observed in PSpice and Silvaco MixedMode is shown in Figures 4-27 and 4-28. Upon applying a gate pulse as input (red wave) to the circuit, the FET acting as a switch is closed allowing current to flow through least resistance path. Corresponding drain voltage, $V_D$ (orange wave), source voltage $V_S$ (green wave) and drain-source voltage $V_{DS}$ (pink wave) during switching is shown.

Upon comparison similar voltage switching ($V_{DS}$) of GaN FET is observed in experimentally measured results and the simulated device results of both PSpice and Silvaco MixedMode. This shows that the experimentally measured
device, manufactured device and modelled device are all in close relation to each other.

For the experimentally measured circuit, it is observed that the $V_{DS}$ rising more than 40V in 4nsec (Figure 4-29), as $V_{DS}$ (pink waveform) represent 40V/div and each division 5nsec. The $dv/dt$ which is induced in the circuit is around 10V/ns.

4.3.4 Simulation of Device switch ON time

In real life, ideal square wave cannot be realized. So in order to better simulate the device response, a square wave generated from a square wave generator is imported into SILVACO and given as the input gate pulse. The

Figure 4-29: Zoomed in image during switching
amplitude of the generated square wave is set to be 3V and its pulse width is set to be 3µ sec.

In Figure 4-22, a transient response of gate voltage and drain current is plotted. The green waveform denotes the imported square wave along with the wave harmonics like overshoot, undershoot and ringing. The corresponding drain current obtained is multiplied 1000 times to be able to see voltage and current in the same graph. The scale towards the left measures the voltage in volts, while the scale towards the right depicts the current in amperes.

Figure 4-30: Transient response of Gate voltage along with output drain current for GaN based HEMT
Figure 4-31: Device switch ON time for physically modelled GaN based HEMT

The above Figure shows the device turn ON transit. It shows us the speed at which the modelled GaN FET switches from OFF state to ON state. It is basically the time taken to transfer the charge from gate terminal to switch ON the FET. Also, the switching speed can be further controlled by connecting a series resistance to the DUT.
4.4 Single Event Effects (SEE)

Any event which disrupts the normal behavior of a circuit due to radiation particles (nuclear particles, photons, etc.) is called an upset. The need for electronic circuits to be fault free has never been much greater ever since the renewed interest in power devices as high-power solid state switches started. An event is considered a failure mode when a high energetic particles turns ON the power device which is biased in its OFF state [47]. These particles can be a result of cosmic rays, radioactive sources or others.

Experiments have been conducted to study potential destructive events such as Single Event Burnout (SEB) and Single Event Gate Rupture (SEGR). These have been well known to cause failures (experimentally and theoretically) in power MOSFETs [48]. SEB is a sudden catastrophic failure occurring due to passage of heavy ion through the source while SEGR is a similar failure occurring when a heavy ion passes through gate or ruptures gate oxide [49]. However, AlGaN/GaN HEMTs are observed to be immune to SEB but an event similar to SEGR is observed [50]. This research also includes testing the effect of heavy ion radiation over AlGaN/GaN devices. By utilizing the ion strike simulation capabilities of SILVACO, we can model the effect of such events on physically modelled AlGaN/GaN power device. Related experimental measurements were performed in our lab by Shams Faruque [44]. AlGaN/GaN
devices (EPC 2001) were examined by connecting 10 of them in parallel and then exposing this test circuit to sun’s radiation for a period of over 240 hours. No SEB failure for the AlGaN/GaN devices was observed. Note that the tested devices did not have any packaging to protect the device from radiation.

The sensitivity of the device to SEE is often estimated by bombarding the DUT with high energy particles [48]. This can been performed in Silvaco by running ion strike simulations with various particle energy densities (we chose to simulate using particle energy density of 20 MeV-cm²/mg upon referring journal paper [48]) on the physically modelled enhancement-mode AlGaN/GaN device structure under biased drain voltage and unbiased gate voltage conditions.

The results depend on several characteristics such as LET (Linear Energy Transfer), range, radius, angle of incidence, radiation duration etc of the ion. In spite of introducing high amount of radiant fluence by Silvaco the device did not breakdown.
Figure 4-32: Single Event Upset simulation. LEFT: At time = 0.5 Pico sec; Right: At time = 2 Pico sec

In Figure 4-24, a Single Event Upset (SEU) is portrayed for a physically modelled AlGaN/GaN HEMT is simulated at time = 0.5 Pico seconds and time = 2 Pico seconds respectively. In this simulation, a single event having a pulse width lasting 0.5 Pico seconds was applied to a powered GaN HEMT when the device was in enhancement mode.
The transient SEU simulation revealed that the DUT got switched ON for a short duration of 3ns even though the SEU lasted for only 0.5 Pico seconds. We need to further study, the sensitivity of the tested power GaN HEMT towards alpha particles (ion strikes), as there might be recoil reaction within the devices.
4.4.1 Effect of induced interface charge

The GaN structure modelled in Silvaco is immune to single event effects. However, experimental results show that whenever a beam of blue laser light is illuminated over a GaN device, while $V_G$ is below threshold voltage and a significant $V_{DS}$ is applied relatively, a sudden increase in drain current is observed [44]. A possible explanation of this kind of effect could be due to formation of charge layers due to release of electrons from generated traps in the AlGaN/GaN HEMT interface. These traps are caused due to defects in deeper band levels of AlGaN and GaN [51], [52].

To model the effect of interface charge on drain current, a positive charge of $5 \times 10^{13}$ cm$^{-2}$ is applied on a P-GaN HEMT (p doped) and a negative charge of $5 \times 10^{14}$ cm$^{-2}$ is applied on a Schottky GaN HEMT (n doped).
Figure 4-34: Charge dependence of the drain current for P-GaN HEMT at $V_{GS} = 0V$ and $V_{DS} = 30V$

A series of charge concentration has been applied at the AlGaN interface of P-GaN HEMT; it is observed that a raise in drain current has been noticed for charge concentrations starting from $+1 \times 10^{13}$ cm$^{-2}$. A plot with a charge concentration of $+5 \times 10^{13}$ cm$^{-2}$ is illustrated in Figure 4-34 above. Red waveforms represent a plot with excess induced charge, while black waveform represents a plot without any additional charge.
It is observed that placing induced interface charges in AlGaN layer increases the leakage current of GaN FET while the device is below threshold voltage. Furthermore, it has been noticed that charge concentrations starting from $-1 \times 10^{13}$ electrons cm$^{-2}$, observe a raise in drain current for a Schottky GaN HEMT device structure. A plot with a charge concentration of $-5 \times 10^{14}$ electrons cm$^{-2}$ is illustrated in Figure 4-35 above. Red waveforms represent a plot with excess induced charge, while black waveform represents a plot without any additional charge.
4.4.1.1 I-V characteristics with observed latching

Light induced carrier trapping is a critical property that can’t be overlooked to avoid drain current leakage losses. To test the carrier trapping in HEMTs, we have experimentally measured the I-V characteristics of GaN HEMT (EPC 2001) with and without blue laser light as it was previously observed to affect the leakage current [44].

![Graph showing I-V characteristics with and without blue laser light](image)

Figure 4-36: Experimentally measured I-V characteristics with/without blue laser light

The Figure 4-36, latching behavior is observed for EPC 2001 when a blue laser is shined upon it. The black waveform (the lower curve of the two) represents the
regular I-V characteristics at gate voltages of 2V and 3V, while blue waveform represents the I-V characteristics with blue light shinned upon it at gate voltages of 2V and 3V respectively.

![I-V characteristics of modelled P-GaN HEMT](image)

Figure 4-37: Experimentally measured I-V characteristics with/without induced additional charge

In Figure 4-37, we observed a similar latching behavior in the modelled P-GaN HEMTs when an enough charge ($+1 \times 10^{13} \text{ cm}^{-2}$) is placed at the interface of AlGaN layer. This gives us a reason to believe that positive charge carriers are getting trapped under the gate terminal in P-GaN HEMT which increases the amount of drain current flowing through the device. The black waveform (the lower curve) represents the regular I-V characteristics at gate voltages of 2V and
3V, while blue waveform (the upper curve) represents the I-V characteristics with added positive charge at the interface while measuring gate voltages of 2V and 3V respectively.

Figure 4-38: I-V characteristics before and after stress caused by excess positive charge for gate voltages of 0 to 5V in a P-GaN HEMT. (Silvaco simulation)

To have a sense of completion, a full I-V characteristic is illustrated in Figure 4-38, before and after an excessive charge of $+1 \times 10^{13} \text{ cm}^{-2}$ is induced in to the AlGaN layer of Silvaco modelled P-GaN HEMT. Red waveforms represent a plot with excess induced charge, while black waveform represents a plot without any additional charge.
Chapter 5  Conclusions and Future Work

In this thesis, we have simulated physically based AlGaN/GaN HEMT structures using Silvaco ATLAS. From the device models the performance characteristics of these power transistors have been extracted. The effort has been focused on parameters such as 2DEG, doping profile, gate work-function, polarization, mobility, temperature and recombination.

Leakage current is known to significantly degrade the performance of GaN devices, hence it needs to be limited. Temperature-dependent simulations revealed that the leakage current in GaN devices increased almost exponentially with the rise in temperature.

Based on the measured data, we compared device performance of modelled AlGaN/GaN HEMTs with that of commercially available GaN devices, through study of I-V characteristics, thermal device performance (HTRB), circuit simulation and Single Event Effects.

It has been reported that, based on simulations, GaN HEMTs have high immunity towards destructive single event effects such as heavy ion radiations, and this was observed by several groups upon testing of actual devices.
Furthermore, addition of charge at the AlGaN interface in order to model the formation of light-induced trapped carrier charge was modelled in order study the dependence of GaN device performance and specifically, the sensitivity of drain current to such effects. It was observed that the device could turn ON before its threshold region when a sufficient amount of charge is applied, which could explain the experimentally observed switching (latching) of off-state devices under blue laser light irradiation.

Overall, the simulation models and experimental testing reveal that GaN based HEMTs perform well in high power, high temperature and high frequency applications due to their high breakdown voltage, high electron velocity, low leakage current and high thermal stability characteristics.

5.1 Future work

Although the results presented in this thesis are promising, further study should be focused towards other reliable techniques to further reduce the effect of surface traps induced near the gate terminal in HEMTs. Additionally, study should be focused pointing to design engineering of field plates, as they have the capability to reduce current collapse and maximize the frequency performance. Nonetheless, research should be improved in designing high powered HEMTs for higher power applications.

Though GaN based HEMTs have showed outstanding performance capabilities, it is far from reaching its theoretical limits of performance.
References


Appendix A

Atlas statements syntax

Specifying Initial Mesh

Defining a device structure involves the aforementioned steps. For instance, specifying an initial mesh involves a series of horizontal and vertical lines and spacing between them. The command language must have the following syntax:

\[
X.MESH\; LOCATION=<VALUE>\; SPACING=<VALUE>
\]

\[
Y.MESH\; LOCATION=<VALUE>\; SPACING=<VALUE>
\]

Specifying Regions and Materials

Over the defined mesh, every location on the mesh needs to be assigned a material region.

The following is syntax for defining region and material in Atlas:

\[
REGION\; number=<integer>\; <material\_type>\; <position\_parameters>
\]
Specifying Electrodes

Once the regions and materials have been specified, the electrode position connecting the semiconductor material need to be specified. This is done using the electrode statement.

\[ \text{ELECTRODE NAME=<electrode name> <position\_parameters>} \]

Specifying Doping

Two common doping distributions for the device structure can be specified using Atlas which are

- Uniform doping profile
- Gaussian doping profile

The following are their respective syntax:

\[ \text{DOPING UNIFORM CONC=<value> N.TYPE REGION=<number>} \]
\[ \text{DOPING GAUSSIAN CONC=<value> P.TYPE CHARACTERISTIC=0.05} \]
\[ <\text{position\_parameters}> \text{PEAK=<number>} \]

Specifying Material properties

Though all the defined materials use the default parameters initially, you can specify your own basic parameters to be used for solving the model. The following is example syntax:

\[ \text{MATERIAL MATERIAL=<material name> EG300=<value> MUN=<value>} \ldots \]
Note that not only EG300 and MUN but several other material properties like TAUN, TAUP, NC300 etc. can be mentioned in the above syntax.

**Specifying Interface Properties**

The INTERFACE statement is used to define the interface charge density and surface recombination velocity at interfaces between semiconductors and insulators. For example, the statement:

```plaintext
INTERFACE QF=<value>
```

Is used to specify the fixed charge between semiconductors and insulators.

**Specifying Physical Models**

Physical models are specified using the MODELS and IMPACT statements. These physical models are grouped into five classes: mobility, recombination, carrier statistics, impact ionization, and tunneling based on which the model statements are used.

For example, the statements:

```plaintext
MODELS CONMOB FLDMOB SRH FERMIDIRAC
IMPACT SELB
```

Specifies that the standard concentration dependent mobility, parallel field mobility, Shockley-Read-Hall recombination with fixed carrier lifetimes, Fermi
Dirac statistics and Selberherr impact ionization models will be used to simulate this model.

**Specifying Numerical methods**

Numerical methods are used to calculate the solutions for the semiconductor device problems. Commonly used numerical methods are NEWTON, GUMMEL and BLOCK. The following is example syntax:

```plaintext
METHOD <Method Name>
```

**Obtaining Solutions**

We can calculate DC, AC small signal, and transient solutions. In all the simulations, the device starts with zero bias on all electrodes. Solutions are obtained by ramping the biases on electrodes from this initial equilibrium condition. These obtained results are saved in log files and finally displayed using EXTRACT and TONY-PLOT statements.
Appendix B

PSpice ideal diode model parameters

*** General Purpose Fast Rectifier ***

.model D1N914  D(Is=168.1E-21 N=1 Rs=.1 Ikf=0 Xti=3 Eg=1.11 Cjo=1p M=.3333
+    Vj=.75 Fc=.5 Isr=100p Nr=2 Bv=100 Ibv=100u Tt=100.0p)

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