Analysis of thermal stress and plastic strain in studs/vias of multilevel integrated circuits

Oluyinka Olugbenga Bamiro
The University of Toledo

A Project

Entitled

ANALYSIS OF THERMAL STRESS AND PLASTIC STRAIN IN STUDS/VIAS OF MULTILEVEL INTEGRATED CIRCUITS

by

Oluyinka .O. Bamiro

Submitted as partial fulfillment of the requirements for

The *Master of Science Degree in Mechanical Engineering*

Advisor: *Dr. Mehdi Pourazady*

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An Abstract of

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The thermo-mechanical reliability of microelectronic circuitry is adversely affected by failure mechanisms such as void formation, interfacial delamination, cracking and electro-migration. The thermal stresses induced during typical integrated circuit fabrication aggravate these failure mechanisms. The high tensile hydrostatic stress is responsible for void nucleation while the individual stress components are responsible for failure mechanism such as void growth, delamination and cracking. The reliability of studs that connects the interconnect from one level to another have been a major source of concern in microelectronic circuitry

A three dimensional elasto-plastic finite element model was used to analyze the thermal stresses and plastic strain in studs/vias. The model determined the effect of geometric parameters used to achieve higher integration on the thermal stress and plastic

strain in aluminum studs. The effects of strain hardening on the thermal stresses and plastic strain of aluminum stud was determined. The implication of the trend towards copper interconnect and low –k dielectric as recommended by the National Technology Roadmap on Semiconductors on thermo-mechanical reliability of studs was explored.

DEDICATION

This thesis is dedicated to my loving girlfriend Yemisi, my brother, sister and my parents for their help, love and support throughout my graduate studies

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

NOMENCLATURE

Symbols

S11	Normal stress in the 1-axis direction
S22	Normal stress in the 2-axis direction
S33	Normal stress in the 3-axis direction
Pemag	Magnitude of plastic deformation
Hydro	Hydrostatic stress
PSE	Plastic strain energy
ESE	Elastic strain energy

CHAPTER 1

INTRODUCTION

1.1 Background and Motivation

There has been miniaturization of integrated circuits in microelectronic circuitry due to higher integration of the components since its advent in the 1960's as predicted by Moore's Law [1]. Moore's Law predicted an exponential growth in the number of components on a single silicon chip. The exponential growth as predicted by Moore has also led to an accompanying doubling of number of transistors on a chip and microprocessor power every 18 months. The miniaturization started with the Small-Scale integration (SSI) to Medium Scale Integration (MSI) to Large-Scale Integration (LSI) to the Very Large Scale Integration (VLSI) and more recently the Ultra Large Scale-Integration (ULSI). The ULSI integrates millions of devices on a single chip as shown in Figure 1. The reduction in size has the advantages of increase in packing density, device speed and higher integration and increase in computing power at a fixed cost.

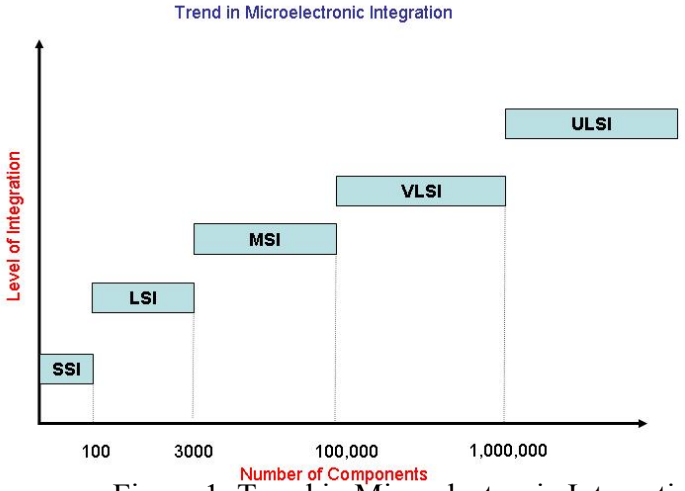

Figure 1: Trend in Microelectronic Integration

A typical integrated circuit contains silicon devices such as transistors which is embedded within the silicon substrate as shown in Figure 2, the metal lines/interconnect conduct the electrical signals to the silicon devices. The number of levels of interconnects determine the level of the integrated circuit, the circuit layout shown in Figure 2 is a two level layout. The studs/vias connect or make electrical contact between two levels of metal line to each other in a multilevel system. The stud and metal assembly are all embedded within a dielectric. The dielectric provides electrical insulation and structural support. Majority of interconnects are made of aluminum but there is a current drive towards using copper because of its lower resistivity relative to that of aluminum, typical studs are usually made of aluminum, tungsten or copper. Dielectrics can either be made of an organic or inorganic material but silicon oxide (SiO_2) an inorganic material is the most widely used material for dielectrics but the trend is changing towards the usage of organic dielectric with dielectric constant lower than that of SiO_2. Reduction in the dielectric constant k leads to a corresponding improvement in interconnects performance because of reduction in parasitic /interlayer capacitance, cross-talk and power dissipation.

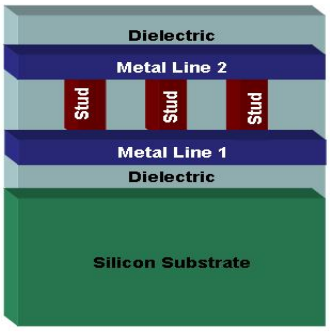

Figure 2a: Two Level Integrated Circuit Layout

The interconnects and studs are usually covered with a thin layer of diffusion barrier layer. Diffusion barrier layers are used to prevent diffusion of interconnect or stud material (Copper or Aluminum) atoms from diffusing into the dielectric or silicon substrate. Typical diffusion barrier layer materials are Titanium Nitride (TiN) and Tantalum Nitride (TaN).

The electrical performance of integrated circuit devices are limited by both transistors and interconnects. The transistor limits the electrical performance through the transistor gate delay while interconnects limits the electrical performance through the interconnect signal delay. The transistor gate delay is proportional to the the size of the transistors while interconnect signal delay is proportional to the resistance-capacitance (RC) time constant. The continuing reduction in sizes of microelectronic devices via higher integration has reduced the problem of transistor gate delay The reduction in cross-sectional area of interconnects has led to an increase in the resistance while reduction in interconnect spacing has led to an increase in capacitance [20]. The increase in both capacitance and resistance of the interconnects leads to an increase in the interconnect delay. The current drive as proposed by the National Technology Roadmap on Semiconductors (NTRS) [23] is to replace the presently used materials for interconnects, studs and dielectric with new materials in order to combat interconnect signal delay. Consequently aluminum is being replaced with Copper while SiO_2 is replaced by low-k polymer based materials. Copper reduces the resistance while low-k dielectrics reduces the parasitic capacitance.

The drive towards increasing the electrical performance of microelectronic devices has adverse effects on the thermo-mechanical reliability. The shrinkage in size of

devices has led to an accompanying reduction in the dimensions of interconnect and vias which aggravates the problem of stress induced void formation and electro migration. Stress induced void formation and electro migration is a threat to the reliability of microelectronic devices. The stress induced void formation is caused mainly by the high thermal stress induced in the studs/vias and interconnects during fabrication process when the whole structure is cooled from fabrication temperature (dielectric or passivation deposition temperature) to room temperature. The induced high thermal stresses in the vias and metal lines are due to the thermal expansion mismatch between interconnect (typically aluminum), via and its surrounding dielectric (silicon oxide in most cases) and the silicon substrate materials.

Extensive research has been done to study the thermal stresses in interconnects but limited research have been geared towards the thermal stresses induced in the studs which suffer a much higher failure rate than the metal lines. The induced thermal stress is useful in studying the micro mechanism of void formation and growth in studs. The changes in material choice as recommended by NTRS to combat signal delay will play a key role in the thermal stresses generated in studs. Higher integration in microelectronic circuitry will also affect geometric parameters (such as stud aspect ratio, line spacing ratio) will be affected. These geometric parameters will have its own effect on thermal stresses generated in studs. The assumed plasticity model will also affect the thermal stresses. Based on these issues, the motivation of this project is to analyze the induced thermal stresses and accompanying plastic strain in studs with variation in plasticity model, material choice and geometric parameters.

1.2 Literature Review

Stress induced voiding in metal interconnects for microelectronic devices had been reported in the early eighties. Since then extensive research has been done to investigate the thermal stresses in metal interconnects to gain further understanding of the mechanism of void nucleation and its growth in microelectronic circuitry. The method of analysis can be divided into three broad categories namely the experimental, analytical and the finite element method (FEM) [2-6, 8-10] . The experimental method employs the wafer curvature, x-ray diffraction techniques. The analytical method [7, 11-14] uses the Eshelby's theory of inclusions [15]. The Eshelby's theory considers an inclusion embedded within an infinite isotropic elastic matrix .The inclusion is a region contained within the matrix with inelastic stress-free strain termed as eigenstrain [14]. The eigenstrain has a finite value within the inclusions but zero outside and the eigenstrain can include thermal strain, phase change strains etc. In microelectronic circuitry, the matrix is the dielectric while the inclusions is the interconnects. In the FEM, the structure is discretized into a finite number of elements with each element having its own stiffness matrix. The element stiffness matrix is then assembled to form the global stiffness matrix. After assembly the resulting equations are solved taking into consideration appropriate boundary conditions. The FEM results have been shown to have good agreement with experimental results [15] and it is often used for determining the thermal stresses in metal lines.

Previous studies have analyzed thermal stresses in only metal interconnects with one level [15-18] or multilevel metallization system [2-4], for periodic metal lines in

staggered and aligned formation [2-4] and variation of stresses with line aspect ratio [5]. Fewer studies have been devoted to thermal stresses in vias/studs that connect the metal lines from one level to another in a multilevel metallization system despite that studs/vias suffer a higher failure rate than the interconnects [2,4,8-9]. The thermal stress in aluminum studs have been investigated using a two dimensional (2D) elasto-plastic FEM model where the aluminum is treated to be elasto-plastic and the other materials were treated as being elastic [2]. The stress in the direction of the height of the stud was the maximum. The normal stresses were observed to have a maximum value at the stud-interconnect interface thereby enhancing failure mechanism in that region [2]. Three-dimensional (3D) elasto-plastic FEM model has been used to study the thermal stresses in studs [8-9] and it was observed that a 2D model of a stud gave similar qualitative results with that of a 3D model but there were pronounced differences in the quantitative results (differences reaching around 300MPa). The difference was attributed to the constraint in one of the dimensions and the three dimensional geometric complexity of the studs [9]. The defective sites or failure regions in the 3D model of the stud were observed to be the stud/dielectric interface and reentrant corners. The defective sites were observed to have good correlation with stress concentration centers. The tensile hydrostatic concentration center is responsible for nucleation of voids. Voids were assumed to nucleate when the tensile hydrostatic stress component is very close to or higher than the cohesive strength of the stud material/dielectric material. The individual normal stresses components were responsible for anisotropic void growth and cracking.

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1.3 Scope and Objectives

The tensile hydrostatic and three normal stress components in a stud have a correlation with formation of voids and its growth. Thus, it is desirable to have a good understanding of the stresses with emphasis on their variation with geometric design parameters (stud aspect ratio h_s/w_s(see Figures 2b and 2c), line spacing ratio p/w (see Figure 2b)), the material properties of stud, interconnect, dielectric and the assumed plasticity model. Hence the objectives of this project is to determine the

- effects of changes in geometric parameters (stud aspect ratio and line spacing ratio) used in achieving higher density microelectronic circuit on the thermal stresses and plastic strain of studs.
- variation of the stresses and plastic strain in aluminum studs with hardening exponent
- implication on the thermo-mechanical reliability of studs due to changes in material towards low k dielectric, copper interconnects and studs.
- effect of diffusion barrier layer on thermal stresses and plastic strain in studs
- employ a 3D finite element method using the ABAQUS software to achieve the above objectives.

1.4 Project Outline

Finite Element (FE) formulation of the three dimensional structure and its implementation is given in Chapter 2. Chapter 3 describes and discusses the results obtained from the parametric studies. The conclusions and summary are listed in Chapter 4

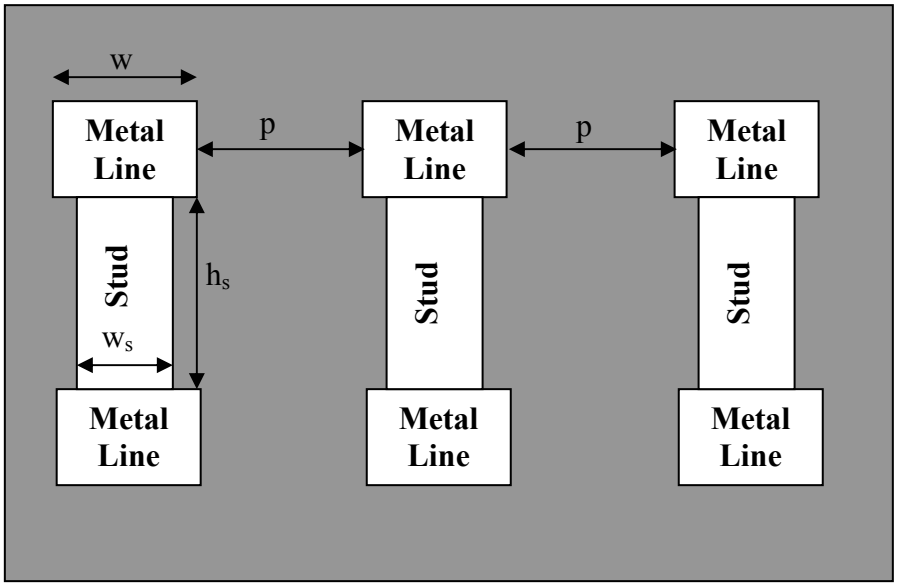

Figure 2b: Two dimensional view of a two level integrated circuit layout

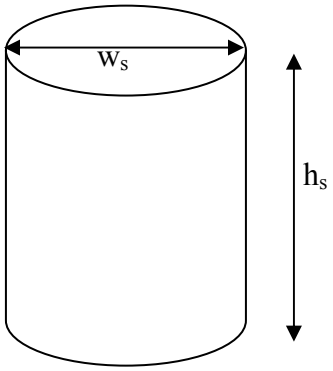

Figure 2c: Three- dimensional view of stud

CHAPTER 2

FINITE ELEMENT MODEL

2.1 Finite Element Method (FEM)

Finite Element Method is a powerful numerical method used to solve multiphysics boundary value problems in engineering. FEM can solve problems in structures, dynamics, electrical, magnetic, heat transfer, acoustic, fluid mechanics and a host of others. The problem can either be solved separately or in combination once the physics of the problem can be reduced to a set of differential equations with appropriate boundary conditions. The continuum model is discretized into a finite number of elements with each element having some sets of nodes. The elements have a shape function which is a polynomial approximation of the field variable (e.g. temperature, displacement). The accuracy of the results depends on the number of elements and the order of the shape function used. Constitutive and equilibrium equations are applied to each element taking into consideration the loading (thermal, mechanical, magnetic, acoustic etc) and the appropriate boundary conditions. The individual elements are then assembled to form a set of linear equations consisting of the element stiffness matrix, field vector and the force/load vector to form the global stiffness matrix and global force/load vector. The set of linear equations are then solved to obtain the field vector from which other derived results such as stress, magnetic flux and heat flux can be obtained from the field vector based on its corresponding constitutive law. The problem

can either range from a one (1D) to three-dimensional (3D) and can also be nonlinear with regards to material properties, geometry or boundary conditions. A coupled thermo-mechanical finite element modeling was implemented for the microelectronic system modeled. Thermal analysis is first done at each iteration step to determine the temperature distribution in the structure. Based on the temperature calculated in the thermal analysis, the stresses are calculated from the constitutive equation taking into consideration the temperature dependent material properties.

2.2 Finite Element Formulation

The dielectric and the diffusion barrier behaved elastically while the interconnect and stud had an elasto-plastic behavior depending on the type of material used consequently the need for an elasto-plastic finite element model.

2.2.1 Elasto-Plastic Model.

Plastic deformation is an irrecoverable or permanent deformation that occurs when a body is loaded beyond its yield limit. The elastic deformation or strain is recovered upon release of the loading. During plastic deformation, the elastic constitutive equations cannot be used to model the nonlinear stress-strain relationship that occurs during plastic deformation hence a need for an inelastic constitutive behavior. The incremental theory of plasticity will be used in the inelastic finite element formulation. The incremental theory relates increments of stress to increments of strain as opposed to the deformation theory that relates the total stress to strain. The incremental theory is

known to give good results for ductile materials. There are three steps when developing inelastic finite element model namely the yield criterion, hardening and flow rules.

The yield criterion helps in determining the onset of yield that is whether the body is in the elastic zone or plastic zone. A yield function F is associated with a yield criterion. The yield function is dependent on the stresses σ, back stress β that describes the translation of the yield function/surface in the stress space while W_p is the plastic work per unit volume.

$$F(\sigma,\beta,W_p) = 0 \quad (1)$$

dF > 0 (implies that plastic flow is moving out of the yield surface that is loading)

dF<0 (constitute the case of unloading)

dF = 0(neutral loading that is the stress state is moving on the yield surface)

The Von-Misses criterion was used as the yield criterion, the effective stress σ_e will be

$$\sigma_e = (½\ \sqrt{2})\left[(\sigma_x - \sigma_y)^2 + (\sigma_y - \sigma_z)^2 + (\sigma_z - \sigma_x)^2 + 6(\tau^2_{xy} + \tau^2_{yz} + \tau^2_{zx})\right]^{½} \quad (2)$$

at the onset of yield the effective stress σ_e will be equal to the yield stress σ_o. σ_x , σ_y and σ_y are normal stresses in the x,y and z directions while τ_{xz}, τ_{xy}, τ_{yz} are the shear stresses.

The hardening rule determines the changes in the yield function as a result of plastic straining. The changes can be in size of the yield surface or location of the center of the yield surface. The centre location is determined by the back stress β while W_p determines the size. For the case of isotropic hardening, β is zero while for kinematic hardening β is non-zero. The kinematic hardening takes into consideration the effects due to Bauschinger.

$$\beta = \int H\ \{\mathbf{d\varepsilon_p}\} \quad (3)$$

Where H is the slope of the stress versus plastic strain

$$W_p = \int \{\mathbf{d\sigma}\}^T \{\mathbf{d\varepsilon_p}\} \quad (4)$$

$$\{\mathbf{d\varepsilon_p}\} = \{ d\varepsilon_{xp} \;\; d\varepsilon_{yp} \;\; d\varepsilon_{zp} \;\; d\varepsilon_{xyp} \;\; d\varepsilon_{yzp} \;\; d\varepsilon_{zxp} \} \quad (5)$$

$$\{\mathbf{d\sigma}\} = \{ d\sigma_{xp} \;\; d\sigma_{yp} \;\; d\sigma_{zp} \;\; d\sigma_{xyp} \;\; d\sigma_{yzp} \;\; d\sigma_{zxp} \} \quad (6)$$

$$\{\mathbf{d\sigma}\} = H \{\mathbf{d\varepsilon_p}\} \quad (7)$$

The effective plastic strain increment $d\varepsilon_{ef}$ is related to the plastic strain increments by the expression stated below

$$d\varepsilon_{ef} = (1/3\ \sqrt{2}) \left[(d\varepsilon_{xp} - d\varepsilon_{yp})^2 + (d\varepsilon_{yp} - d\varepsilon_{zp})^2 + (d\varepsilon_{xp} - d\varepsilon_{yp})^2 + 1.5\{(d\gamma_{xyp})^2 + (d\gamma_{zyp})^2 + (d\gamma_{xyp})^2\}\right]^{1/2} \quad (8)$$

The flow rule determines the relative magnitudes of the components of the plastic strain increment tensor and relates the stress increments to the plastic strain increments. A plastic potential Ψ (σ, β,W_p) is associated with the flow rule. The flow rule is called associated flow rule if the plastic potential $\Psi(\sigma, \beta, W_p)$ is equal to the yield function $F(\sigma, \beta, W_p)$. The associated flow rule was used in all cases involving plasticity.

$$\{\mathbf{d\varepsilon_p}\} = \{\partial\Psi/\partial\boldsymbol{\sigma}\}\, d\lambda \quad (9)$$

$d\lambda$ is a scalar called the plasticity multiplier.

If S_x , S_y and S_z are the deviatoric stress components defined as

$$\left.\begin{aligned} S_x &= \sigma_x - ((\sigma_x + \sigma_y + \sigma_z)/3) \\ S_y &= \sigma_y - ((\sigma_x + \sigma_y + \sigma_z)/3) \\ S_z &= \sigma_z - ((\sigma_x + \sigma_y + \sigma_z)/3) \end{aligned}\right\} \quad (10)$$

Using the Prandtl-Reuss relation

$$\{d\sigma\} = \{Q\}\, d\varepsilon_{ef} \tag{11}$$

$$\{Q\} = (1.5\sigma_e^{-1})\{S_x \;\; S_y \;\; S_z \;\; 2\tau_{xy} \;\; 2\tau_{yz} \;\; 2\tau_{zx}\} \tag{12}$$

$$\{d\varepsilon_e\} = \{d\varepsilon\} - \{d\varepsilon_T\} - \{d\varepsilon_p\} - \{d\varepsilon_c\} \tag{13}$$

$\{d\varepsilon_e\}$ is the elastic strain increment tensor, $\{d\varepsilon_T\}$ is the thermal strain increment tensor, $\{d\varepsilon_c\}$ is the creep thermal strain increment tensor while $\{d\varepsilon\}$ is the total strain increment tensor.

For the elastic portion

$$\{d\sigma\} = [C]\,\{d\varepsilon_e\} \tag{14}$$

$[C]$ is a 6X6 matrix of material stiffness or the material matrix consisting of 36 constants, for the case of isotropic material properties as encountered in this project the 36 constants reduces to 2 independent constants namely the Young Modulus E and the Poisson's ratio ν.

Substituting the equation (13) into (14) to obtain (15)

$$\{d\sigma\} = [C]\,\left\{\{d\varepsilon\} - \{d\varepsilon_T\} - \{d\varepsilon_p\} - \{d\varepsilon_c\}\right\} \tag{15}$$

Substituting (11),(13) into (15)

$$d\varepsilon_{ef} = [W]\,\{d\varepsilon_{ep}\} \tag{16}$$

$$\{d\varepsilon_{ep}\} = \left\{\{d\varepsilon\} - \{d\varepsilon_T\} - \{d\varepsilon_c\}\right\} \text{ and } [W] = \frac{\{Q\}^T [C]}{H + (\{Q\}^T [C]\,\{Q\}}$$

$$\{d\sigma\} = [C_{ep}]\,\{d\varepsilon_{ep}\} \tag{17}$$

$$[C_{ep}] = [C] - [C]\,\{Q\}\,[W] \tag{18}$$

Equation (17) will now form the constitutive equation for the elasto-plastic problem. When the problem is in the elastic regime or domain $[C_{ep}] = [C]$ (that is $\{Q\}$ and $[W]$

will be equal to zero). The elasto-plastic problem is nonlinear; we construct an element tangent stiffness matrix $\mathbf{[k_t]}$.

$$\mathbf{[k_t]} = \int_v \mathbf{[B]^T\,[C_{ep}]\,[B]}\, dV \tag{19}$$

$$\mathbf{[K_t]} = \Sigma \mathbf{[k_t]} \tag{20}$$

$$\mathbf{[B]} = \begin{pmatrix} \frac{\partial}{\partial x} & 0 & 0 \\ 0 & \frac{\partial}{\partial y} & 0 \\ 0 & 0 & \frac{\partial}{\partial z} \\ \frac{\partial}{\partial y} & \frac{\partial}{\partial x} & 0 \\ 0 & \frac{\partial}{\partial z} & \frac{\partial}{\partial y} \\ \frac{\partial}{\partial z} & 0 & \frac{\partial}{\partial x} \end{pmatrix} \tag{21}$$

$$\mathbf{[K_t]_i\,\{\Delta D\}_{i+1} = \{\Delta R\}_{i+1}} \tag{22}$$

The above equation becomes nonlinear because the tangent stiffness matrix is dependent on the displacement **{D}**. The Newton nonlinear numerical scheme was used to solve the nonlinear equation. Details of the algorithm are explained in subsequent section of this report.

2.2.2 Thermal Model

The thermal model was used to model the heat transfer of the microelectronic circuitry. The heat transfer arises when the structure is cooled from the dielectric temperature (dielectric temperature for SiO_2 was 400^oC while that for the low K dielectric was 450^oC) to room temperature of 20^oC. The temperature distribution obtained

from the thermal analysis will be used in obtaining the thermal strain $\{d\varepsilon_T\}$ and other temperature dependent material properties. All materials considered for the thermal model were assumed to be homogeneous and isotropic. Steady state heat transfer analysis with no heat transfer across the boundary was performed.

Steady state heat transfer equation

The differential equation being modeled is the steady heat transfer equation shown below

$$k(\nabla^2 T) + Q = 0 \quad (23)$$

Where k is the thermal conductivity, T is the temperature and Q is the heat generated per unit volume. Q can arise from Joule heating during operational condition of the microelectronic circuit when electric current is passed through the interconnects. Since this project is concerned with stresses generated during fabrication processes, the heat generated per unit volume Q is zero. The differential equation reduces to Laplace differential equation of the form

$$\nabla^2 (T) = 0 \quad (24)$$

Thermal Boundary Conditions

The first or Dirichlet boundary (that is the temperature prescribed) was prescribed for the whole structure, the dielectric deposition temperature (T_{die}) at the initial step and room temperature (T_∞) at the final step of the analysis.

$$T = T_{die} \text{ at } t = 0 \quad (25)$$

$$T = T_\infty \text{ at } t = \infty \quad (26)$$

The Temperature T is related to the nodal temperature $\{T_d\}$ by the use of interpolating shape function **[N]**

$$T = [N]\{T_d\} \quad (27)$$

$$\{T_\partial\} = [B_\theta]\ \{T_d\} \quad (28)$$

Where $\{T_\partial\}$ is the temperature gradients

$$[B_\theta] = \{\partial/\partial x \quad \partial/\partial y \quad \partial/\partial z\}[N] \quad (29)$$

$$[k_\theta] = \int_v [B_\theta]^T [\kappa] [B_\theta]\, dv \quad (30)$$

Where $[k_\theta]$ is the thermal stiffness matrix and $[\kappa]$ is the material matrix, the thermal stiffness matrix $[k_\theta]$ will be not be constant but will be dependent on the thermal conductivity k which is temperature dependent hence the problem becomes nonlinear.

$$[\kappa] = k\,[1\ 1\ 1] \quad (31)$$

$$[K_\theta] = \Sigma[k_\theta] \quad (32)$$

$$[K_\theta]\ \{T\} = \{0\} \quad (33)$$

2.3 Newton Method for Nonlinear FEM

The nonlinearity for the cases being modeled arises from material nonlinearity (plasticity of some of the materials) and the temperature dependence of some material properties. In nonlinear FEM, the stiffness matrix is dependent on the field variable for example for the elasto-plastic model, the tangent stiffness matrix is dependent on both the displacement and temperature while for the thermal model the stiffness matrix is dependent on the temperature.

The Newton method was used to solve the nonlinear FEM. The Newton method is used in finding solutions to nonlinear equations by taking a Taylor's series approximation. The equations are then solved increments and the residual are minimized until a desired convergence to the solution is reached. Several iterations are done for each increment before convergence is achieved.

If $P(\{\mu\}) = 0$ is the nonlinear problem to be solved where $\{\mu\}$is the field variable to be solved for. The problem is solved in increments and in an iterative manner such that at any point in time

$$P(\{\mu\}_i + \{x\}_{i+1}) = 0 \tag{34}$$

Where $\{\mu\}_i$ is the approximation to the original solution at i^{th} iteration and $\{x\}_i$ is the difference between the exact and approximate solutions. Taking the Taylor series expansion of (34) and neglecting higher order derivatives thereby giving a linear approximation

$$P(\{\mu\}_i) + \left(\frac{\partial P}{\partial \{\mu\}}\right)\{\mu\}_i \{x\}_{i+1} = P(\{\mu\}_i) + V_i \{x\}_{i+1} = 0 \tag{35}$$

Where $-V_i = \left(\frac{\partial P}{\partial \{\mu\}} \right) \{\mu\}_i$ = tangent stiffness matrix or Jacobian matrix

The next approximation to the solution will be

$\{\mu\}_{i+1} = \{\mu\}_i + \{x\}_{i+1}$

The iteration continues until a convergence criterion is reached.

For the case of FEM, $P(\{\mu\}) = 0$ will be the virtual work equation, the tangent stiffness matrix $-V_i = \mathbf{[K_t]_i}$. $\{x\}_{i+1} = \mathbf{\{\Delta D\}_{i+1}}$, the load is increased incrementally and the corresponding increment in displacement is solved for iteratively until convergence is reached

$$\mathbf{[K_t]_i \{\Delta D\}_{i+1} = \{\Delta R\}_{i+1}}$$

After solving the above equation, $\mathbf{\{D\}_{i+1}}$ and $\mathbf{\{R\}_{i+1}}$ are updated as follows

$$\mathbf{\{D\}_{i+1} = \{D\}_i + \{\Delta D\}_{i+1}}$$

$$\mathbf{\{R_{i+1} = \{R_i + \{\Delta R\}_{i+1}}$$

$\mathbf{[K_t]_{i+1}}$ will then be updated based on the new values of $\mathbf{\{D\}_{i+1}}$ and $\mathbf{\{R\}_{i+1}}$

$\mathbf{[K_t]_{i+1}\{\Delta D\}_{i+1} - \{\Delta R\}_{i+1} = \{Z\}_{i+1}}$ = Force residual

Since the Newton method is an approximation, the force residual $\mathbf{\{Z\}_{i+1}}$ will not be equal to zero. A suitable convergence criterion has to be specified in order for the iteration to stop or converge for each increment . For the mechanical model, the following conditions must be satisfied before convergence is achieved

$$\text{Max} \parallel \mathbf{\{Z\}_{i+1}} \parallel \leq 0.005 R_t$$

$$\text{Max}\mathbf{\{\Delta D\}_{i+1}} \leq 0.01\mathbf{\{\Delta D\}_{max}}$$

R_t is the overall time average value of the force over the increment

$\{\Delta D\}_{max}$ is the largest change in the nodal value of **{D}** over the entire increment.

For static and steady state analysis as encountered in this project, a time scale has to be specified only for modeling of the nonlinear effects. The time scale was used for determining the increment size. The automatic incrementation was used for a time period of 1, maximum number of iteration per increment was 100, the minimum increment size was set at 0.00003 while the maximum increment size was set at 1 for all cases considered.

2.4 Physical Model and FEM Implementation

2.4.1 Physical Model

The physical models used in this project was the focus in this section. The first-axis is along the interconnect length direction, second-axis is along the interconnect height direction while the third-axis is along the width direction of the interconnect. Figure 4a shows the 2-3 axis view of the physical model for a three level metallization integrated circuit consisting of interconnects M1, M2 and M3. The contact C connects the interconnect M1 to the silicon devices, the stud S1 connects M1 to M2 while stud S2 connects M2 to M3. The stud and contact are centrally located as shown in Figures 3c and 3d. The studs/contacts considered throughout this project were cylindrical in nature and due to the symmetry condition only half of its geometry was used as shown in Figure 7.

Due to the periodic nature as shown in Figures 3a and 4a, axes x-x and y-y was taken as the axis of symmetry and the resulting structure due to symmetry condition is shown in Figures 3b, 3c, 4b and 4c. Figures 3d and 4d show the zoomed 3D view of the model

Symbol	Definition
p	Periodic spacing between 2 consecutive interconnects on the same level
h	Interconnect height
w	Interconnect width
h_s	Stud/contact height
w_s	Stud/contact width or diameter
L	Entire length of Structure
H	Entire height of Structure
(p/w)	Interconnect/line spacing ratio
(h/w)	Interconnect/line aspect ratio
(h_s/w_s)	Stud/contact aspect ratio

Table 1- Definition of symbols and ratios

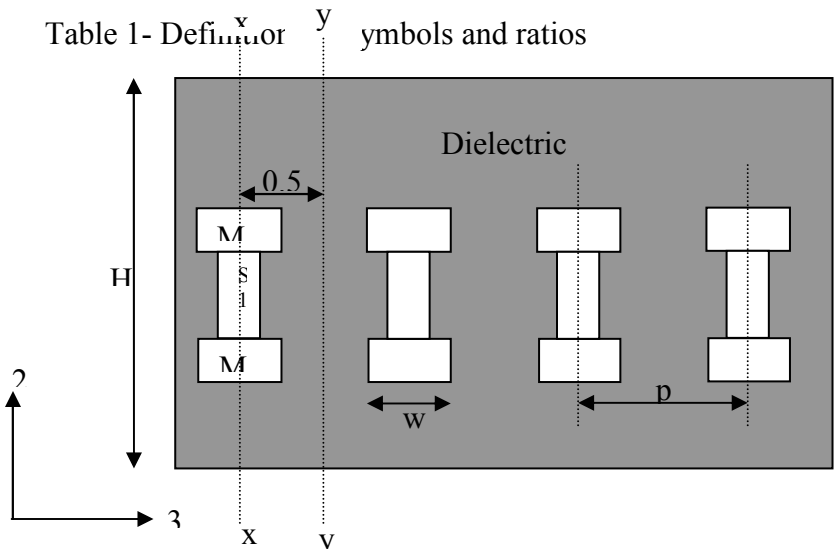

Figure 3a- 2-3-axis view of model used for sections 3.1 and 3.2 before application of symmetry condition

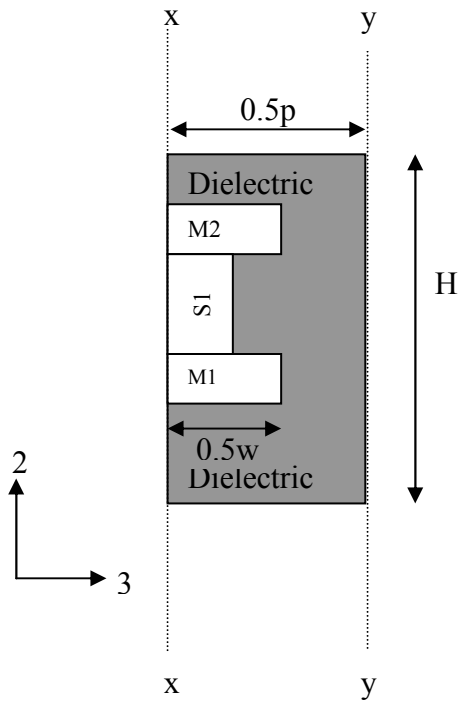

Figure 3b- 2-3-axis view of model used for sections 3.1 and 3.2 after application of symmetry condition

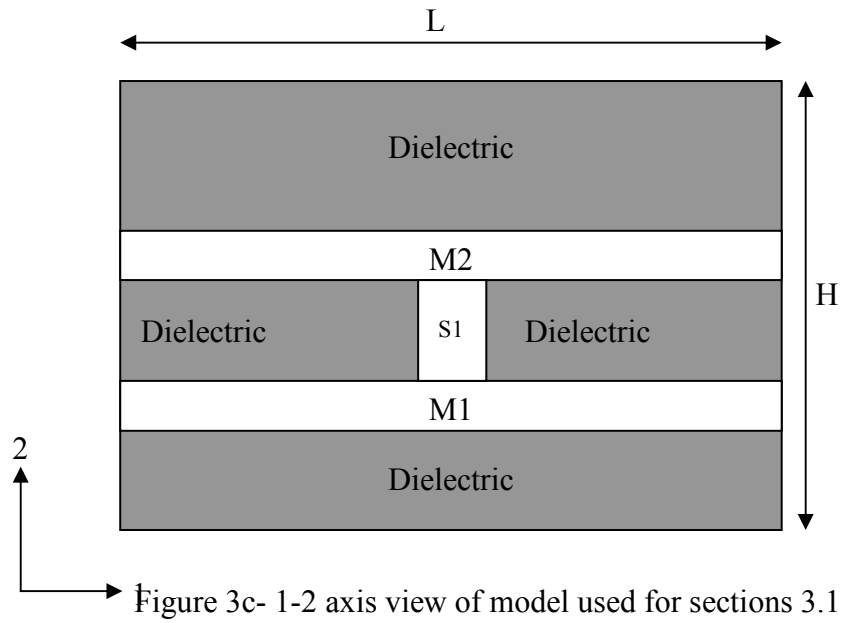

Figure 3c- 1-2 axis view of model used for sections 3.1 and 3.2

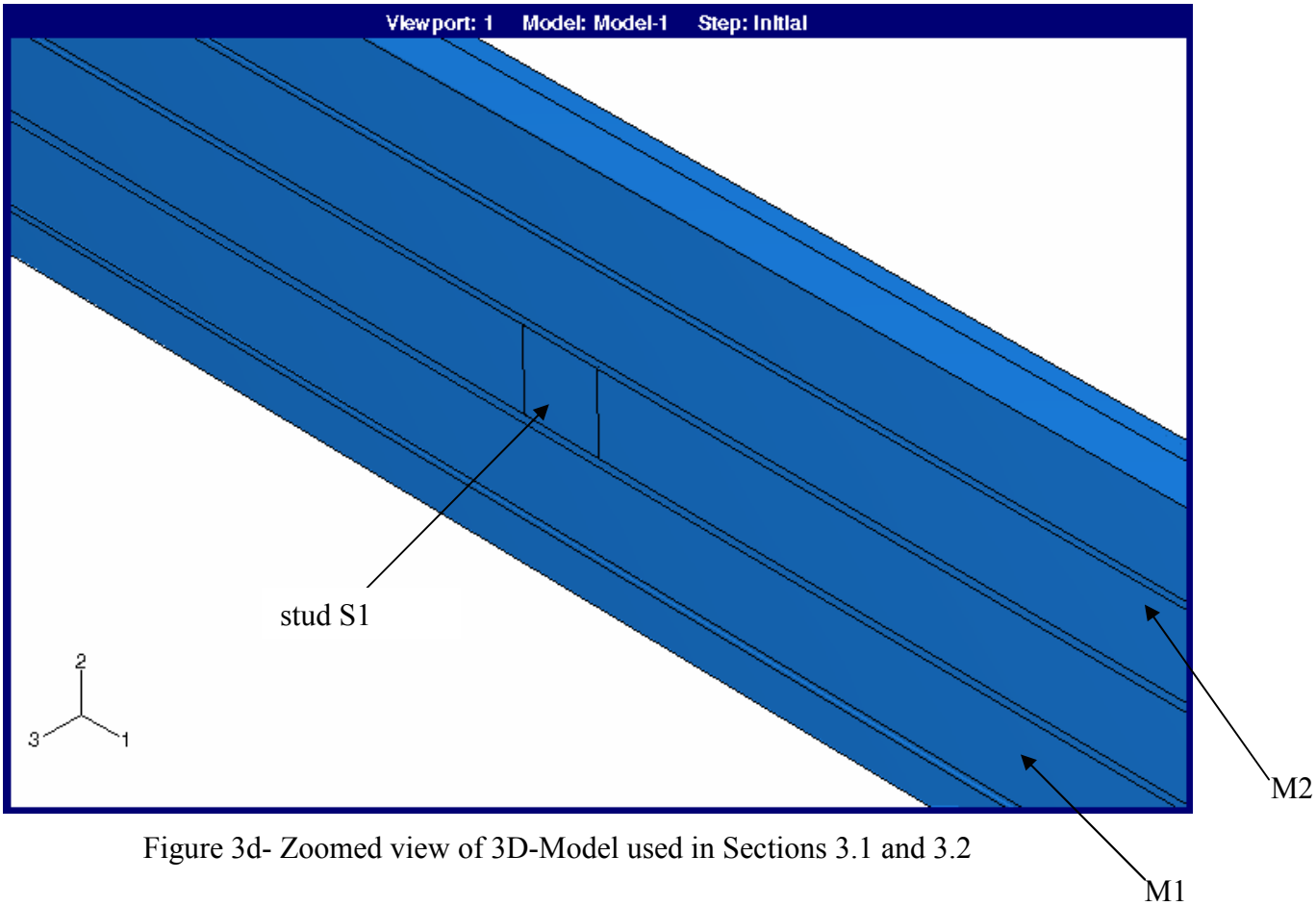

Figure 3d- Zoomed view of 3D-Model used in Sections 3.1 and 3.2

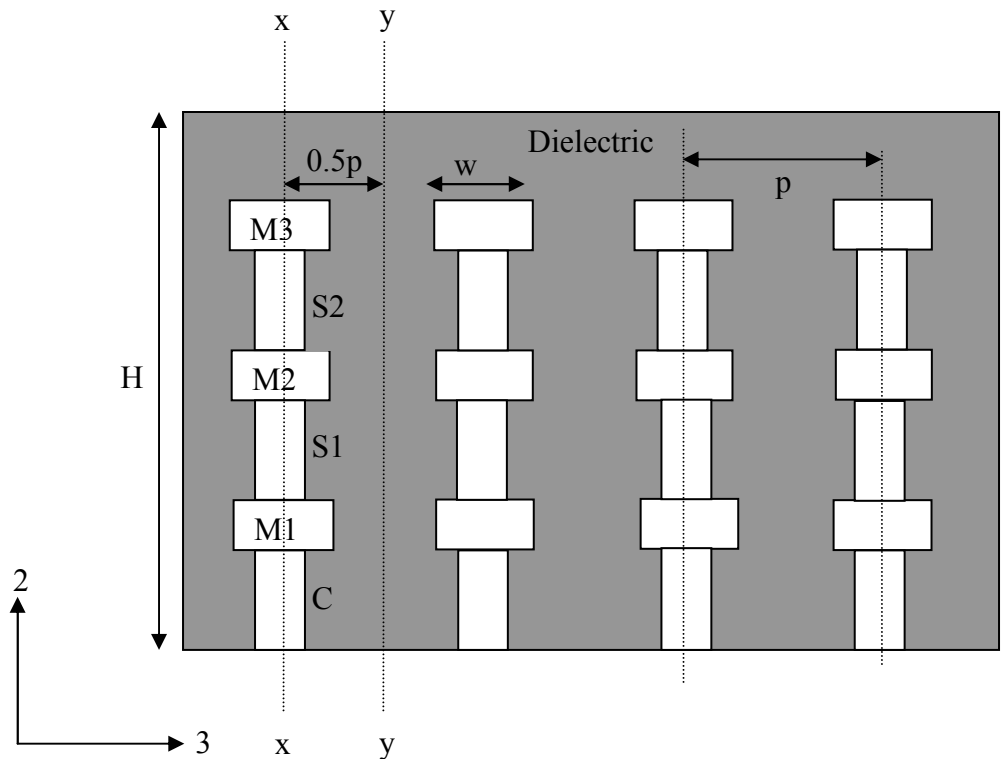

Figure 4a- 2-3-axis view of model used for sections 3.4 and 3.5 before application of symmetry condition

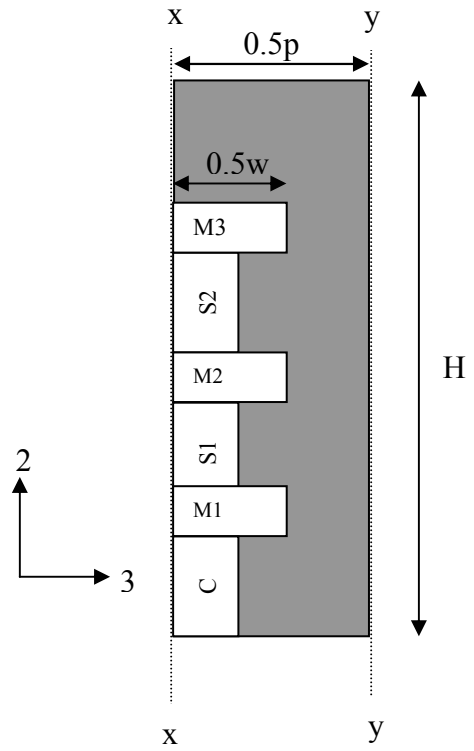

Figure 4b- 2-3-axis view of model used for sections 3.4 and 3.5 after application of symmetry condition

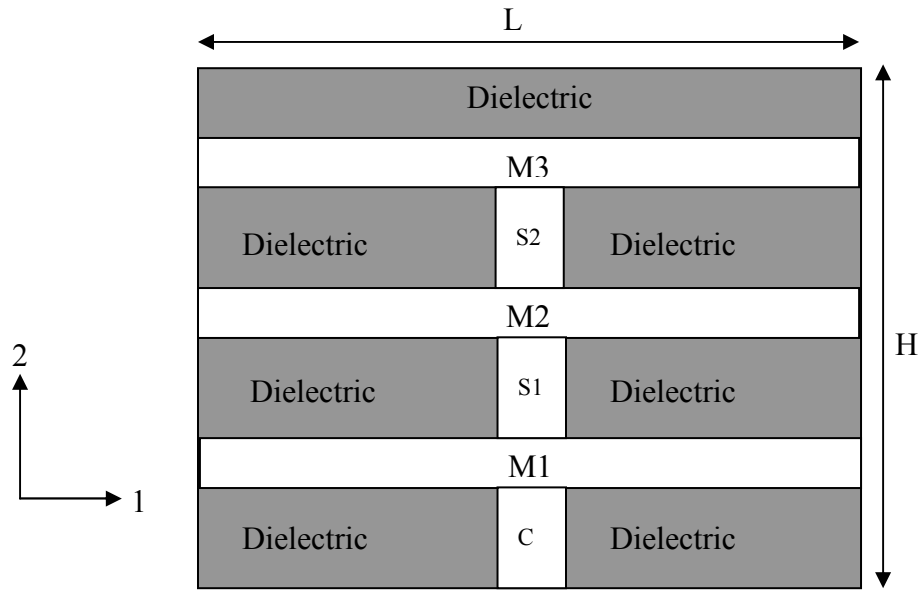

Figure 4c- 1-2 axis view of model used for sections 3.4 and 3.5

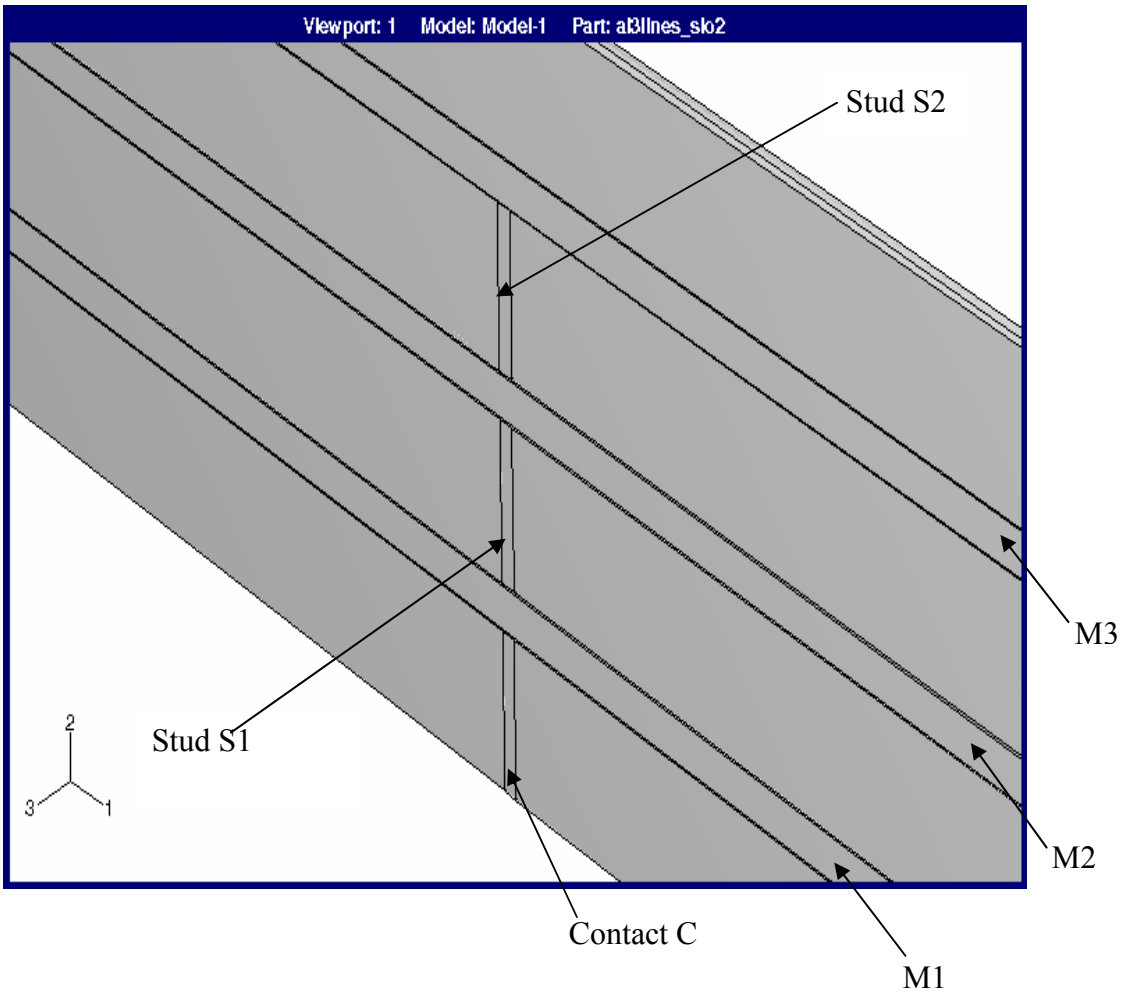

Figure 4d- Zoomed view of 3D-Model used in Sections 3.4 and 3.5

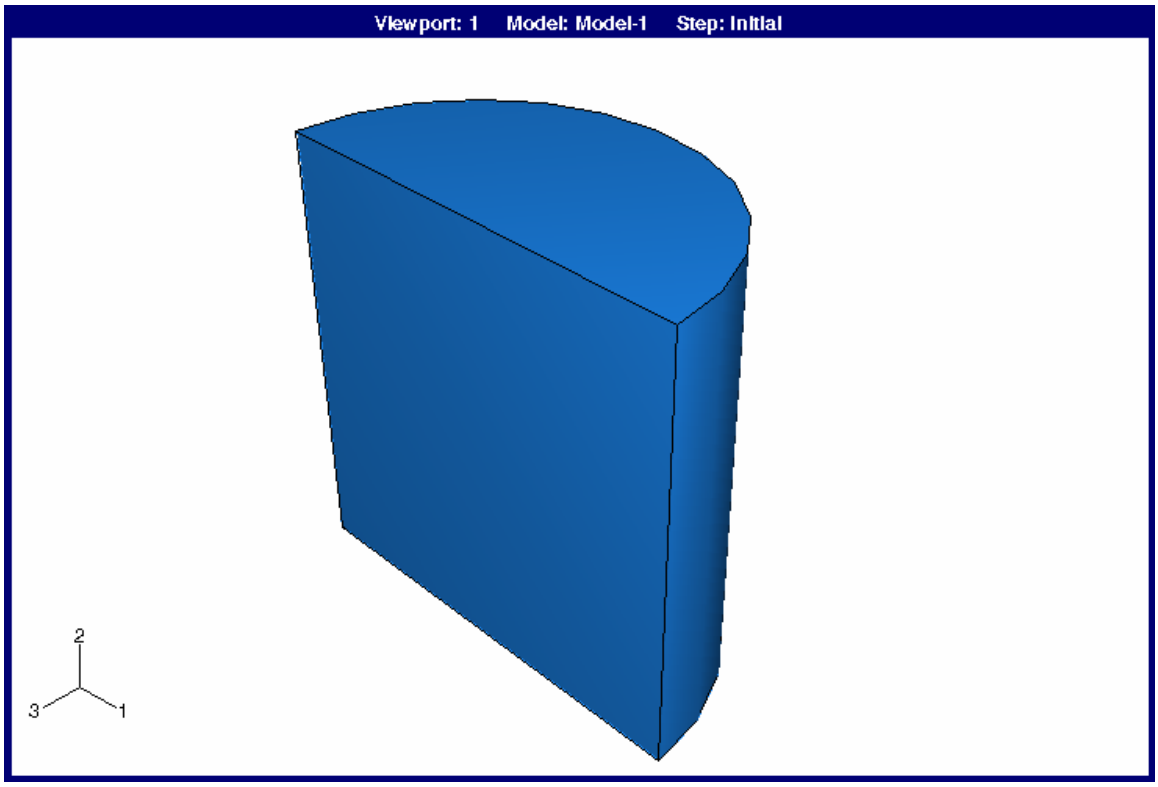

Figure 5- 3D-view of stud and contact used after application of symmetry condition

2.4.2 FEM Implementation

Coupled thermo-mechanical analysis was performed for all cases considered. The materials used for the vias/studs and interconnect lines were aluminum (Al_3), copper (Cu) and tungsten (W). The materials used for the dielectric materials were SiO_2 and SiLK®. SiLK® is a low k (with a dielectric constant of 2.6) dielectric material made by Dow Chemical Company. Titanium Nitride (TiN) was used as diffusion barrier layer for interconnects and studs. Aluminum and copper had elasto-plastic behavior while other materials behaved elastically. Copper exhibited a kinematic hardening behavior with slope H. Aluminum was assumed to have perfectly plastic behavior in some instances and also having a power law hardening behavior when the dependence of stresses with hardening was considered. Table 2 summarizes the material properties of the different materials considered.

The coupled temperature-displacement element C3D8T (shown in Figure 7) was used for all cases considered. C3D8T is a 8-noded trilinear displacement and temperature solid element with four degrees of freedom at the corner nodes (three for displacement **{d}** and one for temperature T_d). Figure 6 shows the meshing of a typical model considered in this project .

	Al_3	Cu	W	SiO_2	SiLK®	TiN
E(Gpa)						
293K	69[a]	110[b]	411[c]	71.4[d]	2.45[e]	470[f]
673K	55[a]	98[b]	411	71.4	2.45	470
723K	53[a]		411	71.4	2.45	470
ν						
293K	0.33	0.3	0.28	0.16	0.35	0.25
673K	0.33	0.3	0.28	0.16	0.35	0.25
723K	0.33	0.3	0.28	0.16	0.35	0.25
$\alpha(10^{-6}/K)$						
293K	23.6[a]	17[b]	4.5	0.52[d]	66	6.5
673K	29.9[a]	19.2[b]	4.5	0.73[d]	66	6.5
723K	30.8[a]	19.5[b]	4.5	0.75[d]	66	6.5
σ_y(MPa)						
293K	200[a]	223[b]	-	-	-	-
673K	67.4[a]	117[b]	-	-	-	-
723K	50[a]					
H(Gpa)						
293K	-	77[b]	-	-	-	-
673K	-	77[b]	-	-	-	-
723K	-	77[b]				

Table 2 Summary of material properties used for FEM

a) Linear variation of E, α and σ_y with temperature (see Ref 4)
b) Cu is assumed to have a kinematic hardening behavior, H is the slope of the stress versus plastic strain and $\sigma_y = \sigma_o(1-T/T_o)$ where σ_o = 305MPa, T_o = 1090K(see Ref 21). The back stress β is calculated by ABAQUS®. E, α are assumed to have a linear variation with temperature (see Ref 21)
c) See Ref 19
d) See Ref 4
e) See Ref 20
f) See Ref 4

Referring to Figure 6, the displacements in second (2) and third (3) axes directions were constrained for the right and left surfaces. Due to symmetry condition, the displacement in the third (3)-axis direction for the front and back surfaces was constrained. The structure is assumed to be rigidly attached to the silicon substrate at the bottom surface hence the displacements in the second and third axes directions were constrained similar to boundary conditions considered in Reference 22. The dielectric deposition temperature T_{die} for SiO_2 was 673K while that for SILK® was 723K

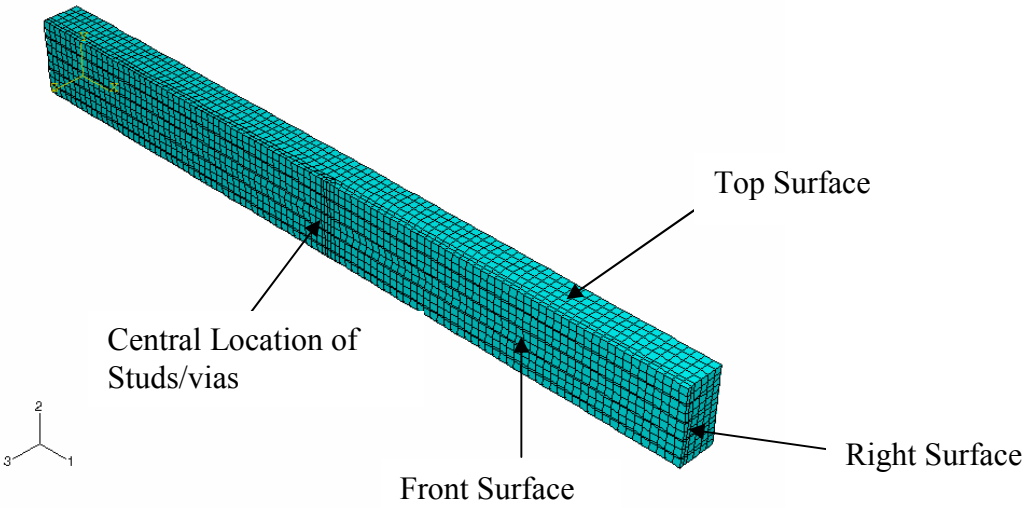

Figure 6- 3D Meshing of Model

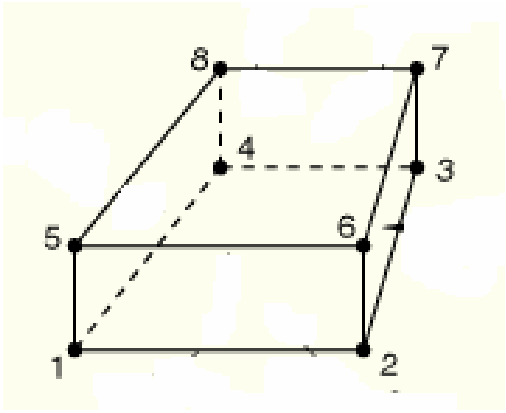

Figure 7- View of C3D8T element used

CHAPTER 3

PARAMETRIC STUDIES

3.1 Effects of hardening on thermal stresses and plastic strain for aluminum stud/via

In reality, no material is perfectly plastic and in many cases there is a considerable amount of plastic strain hardening or work hardening. In most thermal stress analysis of aluminum interconnect structures the assumption of perfectly plastic is usually employed due to the difficulty in obtaining the material properties at the micro-scale level obtained in microelectronic circuitry [2-6].

The aim of this section is to determine the effects of hardening on the thermal stress based on the assumption that aluminum obeys the modified power law [24]. Typically aluminum has a strain hardening index m ranging from approximately 0.1 to 0.25. The trend for studs according to the roadmap [23] is increasing stud aspect ratio due to reduction in the critical dimension (width of stud). In order to achieve higher integration, the line will be closely spaced consequently leading to reducing line spacing ratio p/w. Thermal stresses and plastic strain were analyzed for a two level metallization system as shown on Figures 3a-3d for cases of m equal to 0.1, 0.15 and 0.25.The stud aspect ratio h_s/w_s were 1, 2.5, 4 and 5. The line spacing ratio p/w was 2.5, 3.5 and 5. The stud

aspect ratio was varied by changing the width w_s of the stud while keeping the height h_s. Table 3 gives a summary of the total number of elements used and other geometric parameters used. The interconnects had a TiN diffusion barrier layer thickness of 0.1μm. All outputs that are tabulated are volume averaged

p/w	Number of Elements	H(μm)	L(μm)	h(μm)	w(μm)	h_s(μm)	p(μm)
2.5	5187	4.9	49	1	1	1	2.5
3.5	6448	4.9	49	1	1	1	3.5
5	7776	4.9	49	1	1	1	5

Table 3- Summary of parameters used for sections 3.1 and 3.2

m = 0 (perfectly plastic)					
h_s/w_s	***S11(MPa)***	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
1	512.53	587.7	510.055	536.7617	0.00502
2.5	568.44	665.535	570.78	601.585	0.010485
4	536.88	634.335	534.215	568.4767	0.011587
5	534.385	631.71	531.215	565.77	0.011798
m = 0.1					
h_s/w_s	***S11(MPa)***	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
1	512.73	593.88	508.84	538.4833	0.004694
2.5	562.535	674.855	565.89	601.0933	0.009871
4	531.395	645.1	528.95	568.4817	0.010959
5	529.05	642.8	526.015	565.955	0.011173
m = 0.15					
h_s/w_s	***S11(MPa)***	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
1	511.98	597.015	508.25	539.0817	0.004531
2.5	559.495	679.9	563.44	600.945	0.009551
4	528.54	650.975	526.27	568.595	0.010627
5	526.27	648.86	523.355	566.1617	0.010842
m = 0.25					
h_s/w_s	***S11(MPa)***	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
1	510.495	603.315	507.115	540.3083	0.004212
2.5	553.37	690.625	558.615	600.87	0.008899
4	522.685	663.625	520.88	569.0633	0.009938
5	520.54	661.925	517.995	566.82	0.0101528

Table 4 – Thermal stresses and plastic strain for p/w = 2.5

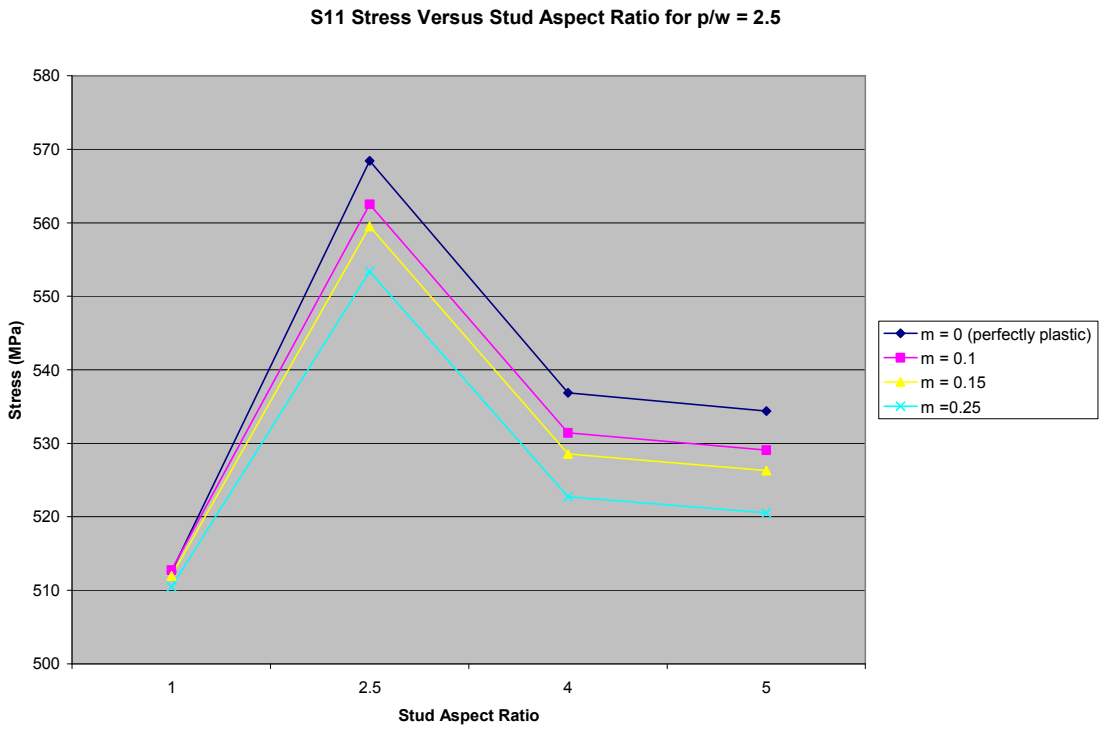

Figure 8- S11 stress for p/w =2.5

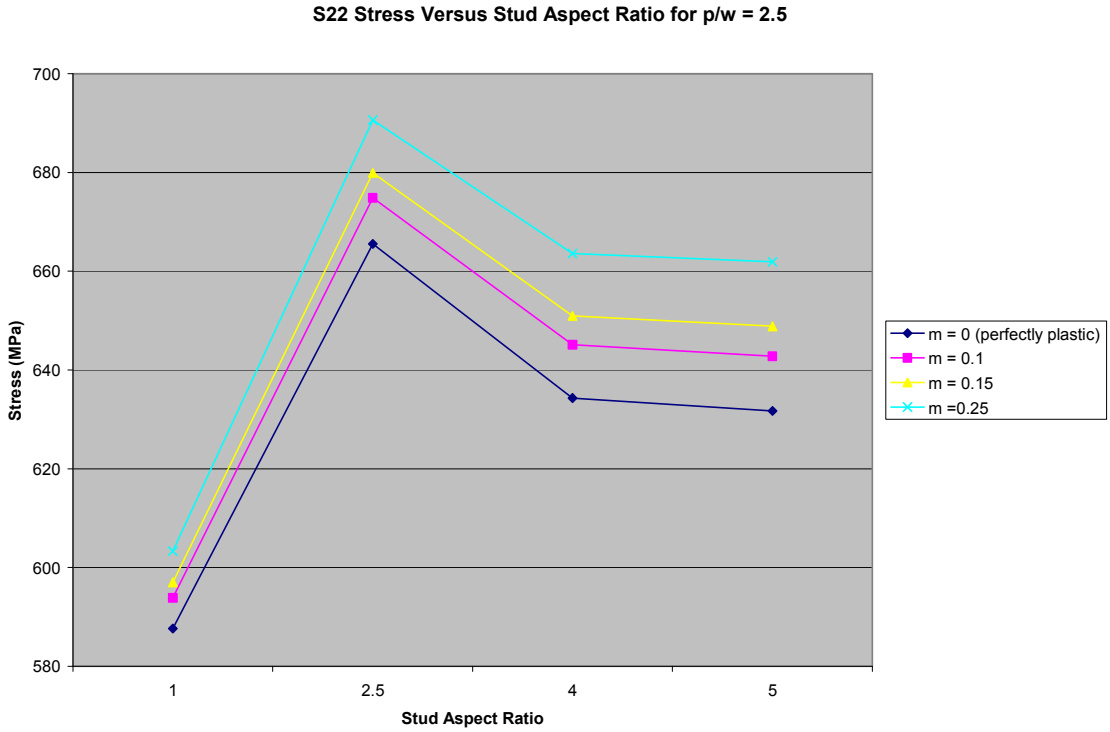

Figure 9- S22 stress for p/w =2.5

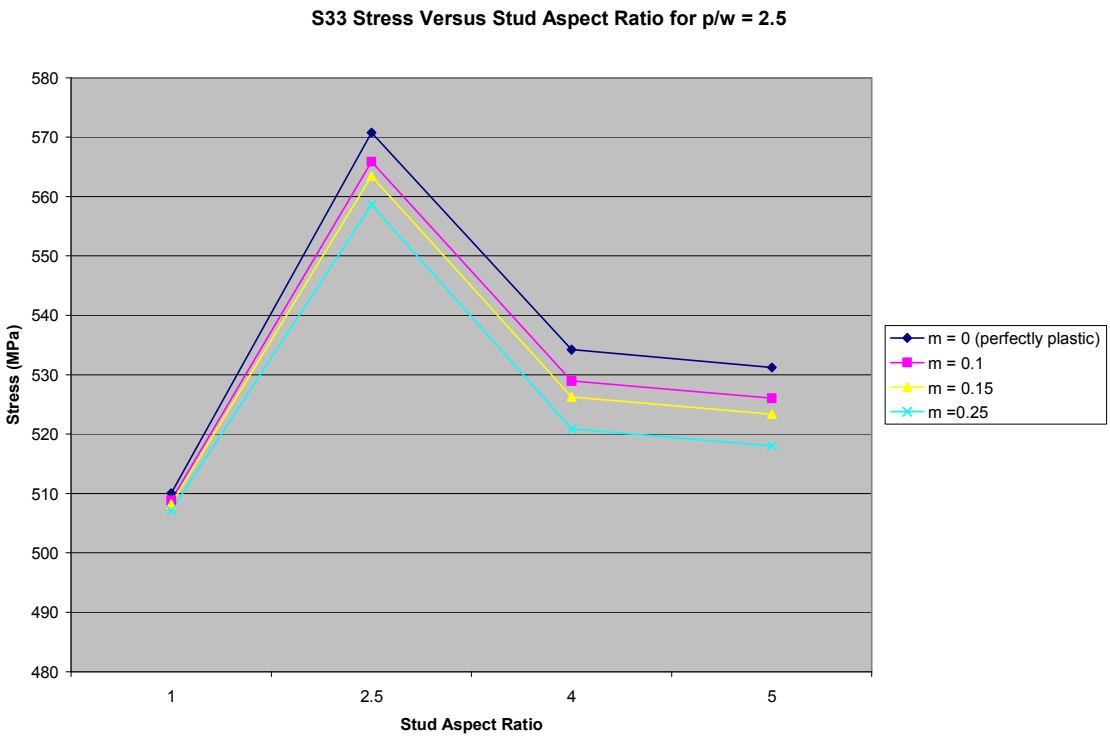

Figure 10- S33 stress for p/w =2.5

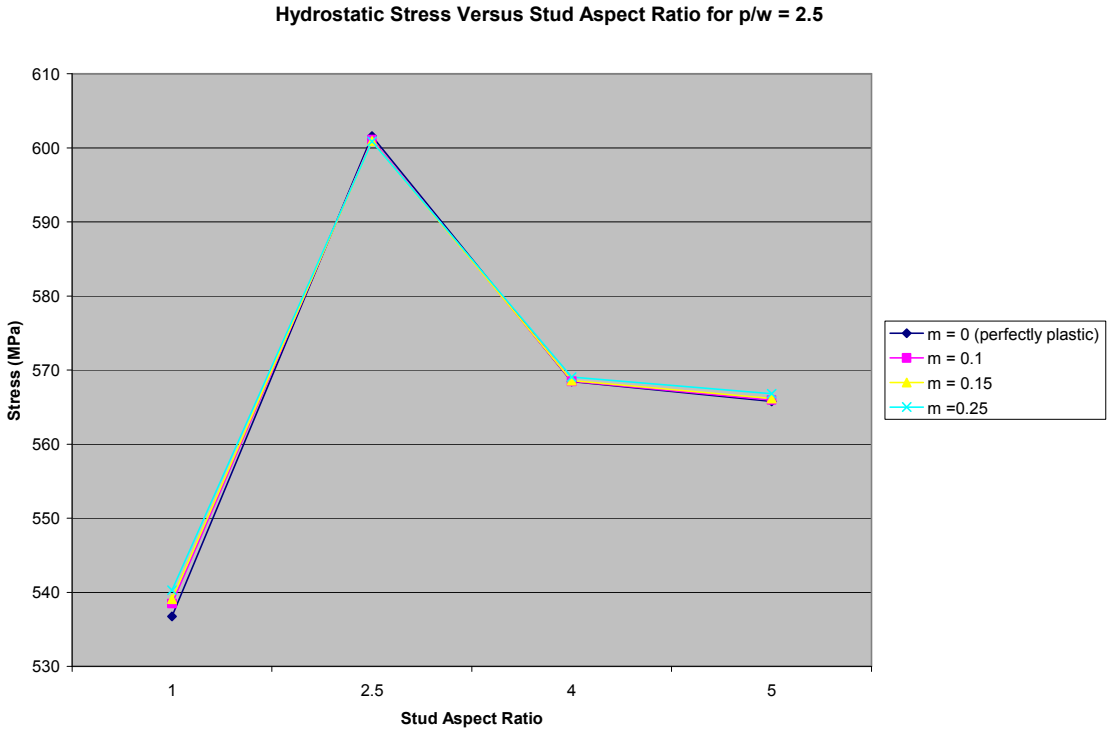

Figure 11- Hydro stress for p/w= 2.5

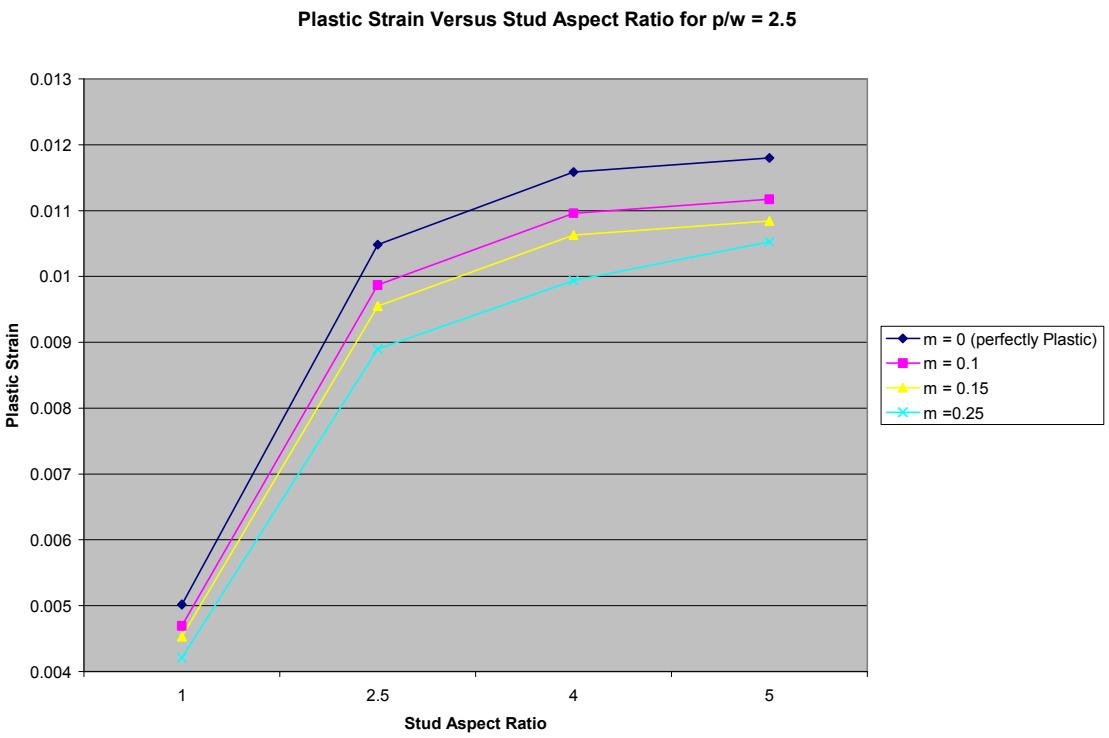

Figure 12- Pemag for p/w =2.5

m = 0 (perfectly plastic)					
h_s/w_s	***S11(MPa)***	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
1	542.519	610.901	519.02	557.48	0.00644
2.5	590.225	682.51	582.54	618.425	0.01144
4	556.87	649.315	544.97	583.718	0.01251
5	554.145	646.53	541.95	580.875	0.01269
m = 0.1					
h_s/w_s	***S11(MPa)***	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
1	541.936	618.674	516.431	559.014	0.00605
2.5	585.65	693.16	577.17	618.66	0.01082
4	552.705	661.275	539.275	584.418	0.01188
5	550.115	658.79	536.335	581.747	0.01207
m = 0.15					
h_s/w_s	***S11(MPa)***	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
1	541.631	622.682	515.125	559.813	0.00585
2.5	583.295	698.975	574.425	618.898	0.0105
4	550.53	667.83	536.325	584.895	0.01154
5	548.01	665.51	533.415	582.312	0.01173
m = 0.25					
h_s/w_s	***S11(MPa)***	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
1	541.003	630.833	512.518	561.451	0.00545
2.5	578.54	711.5	568.92	619.653	0.00983
4	546.075	682.025	530.315	586.138	0.01084
5	543.685	680.08	527.45	583.738	0.01104

Table 5 – Thermal stresses and plastic strain for p/w = 3.5

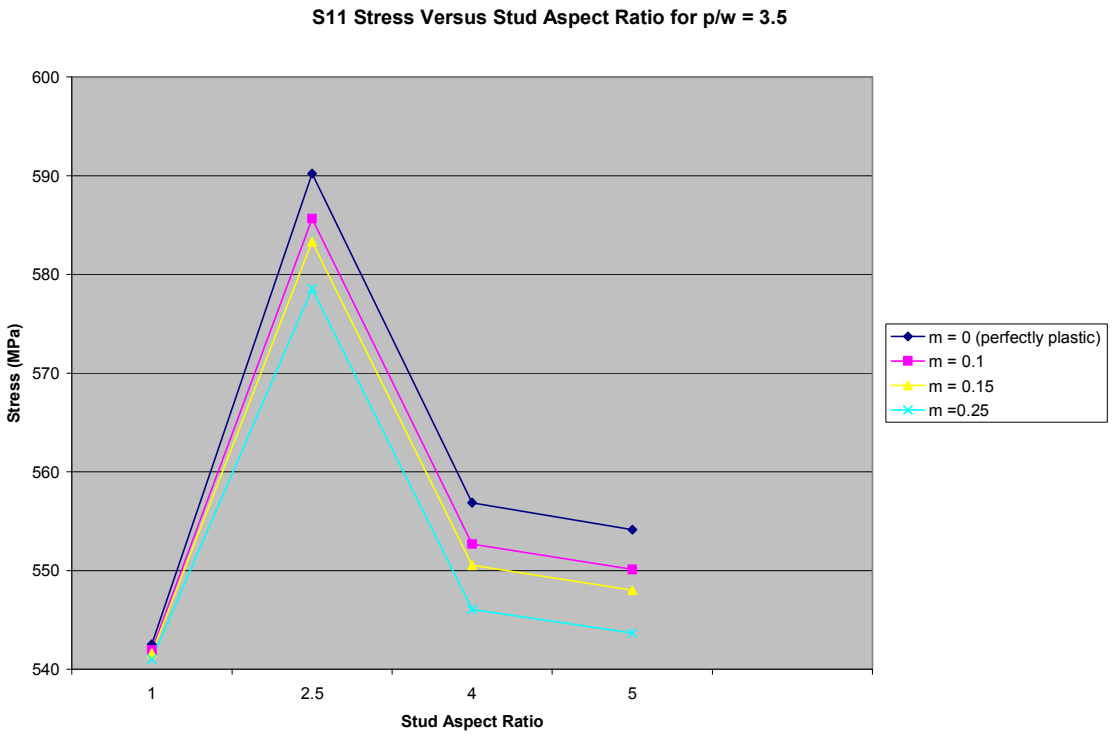

Figure 13- S11 stress for p/w =3.5

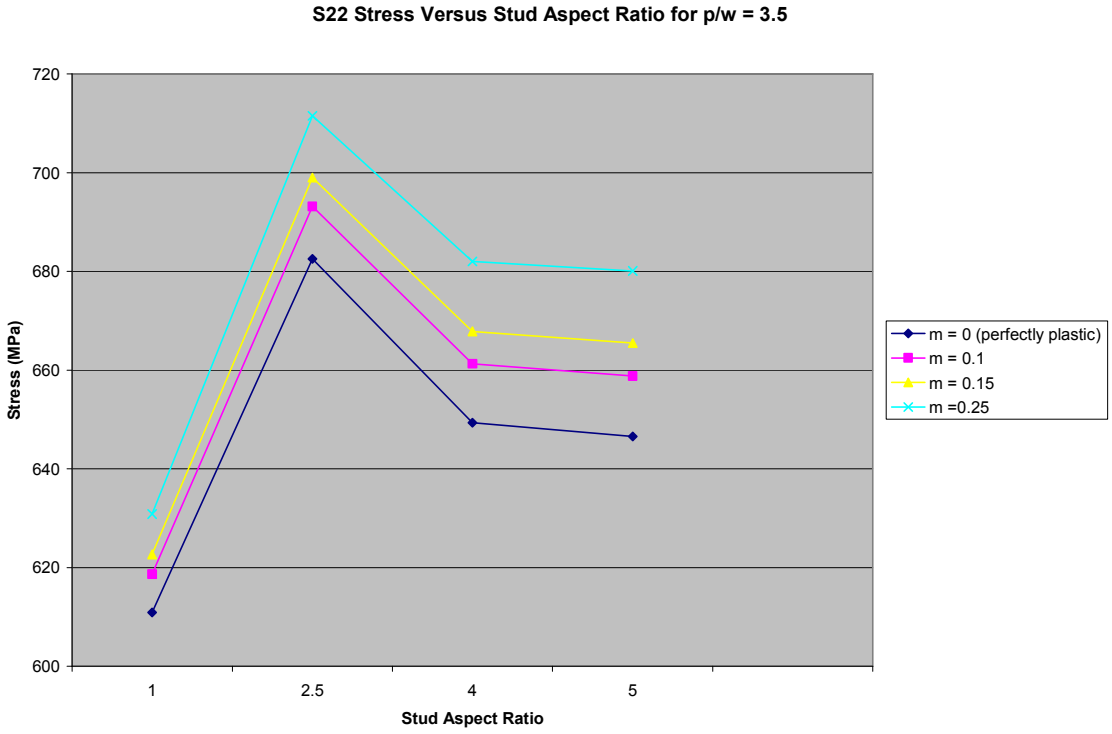

Figure 14- S22 stress for p/w =3.5

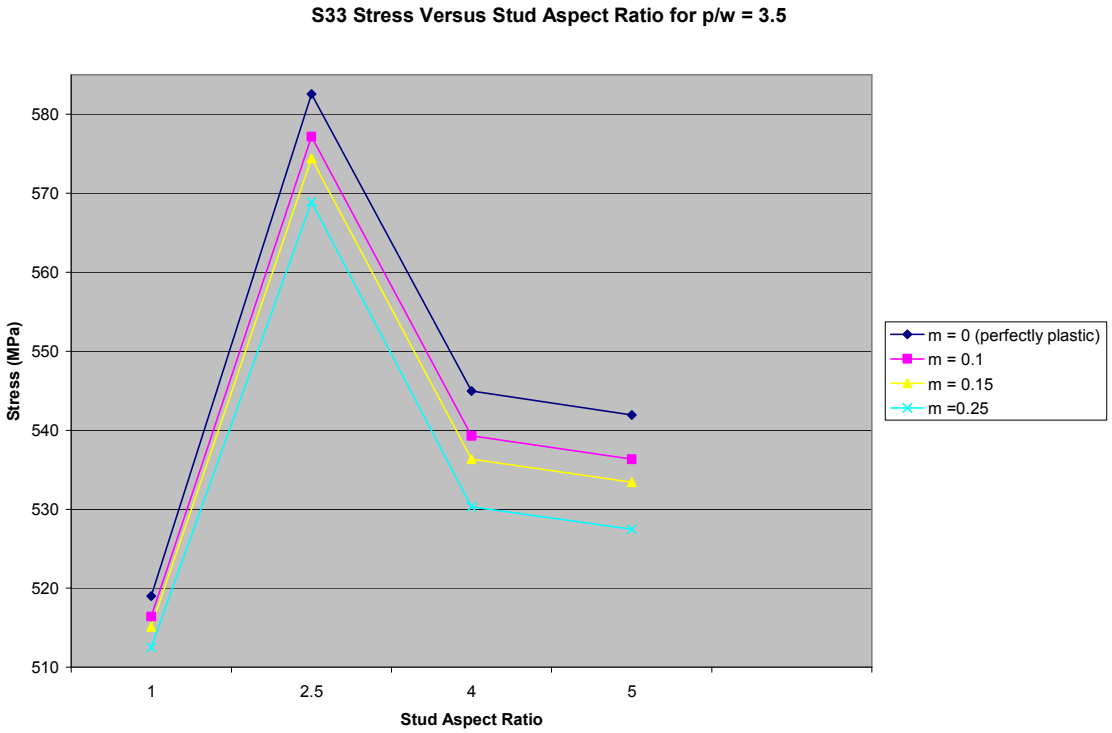

Figure 15- S33 stress for p/w =3.5

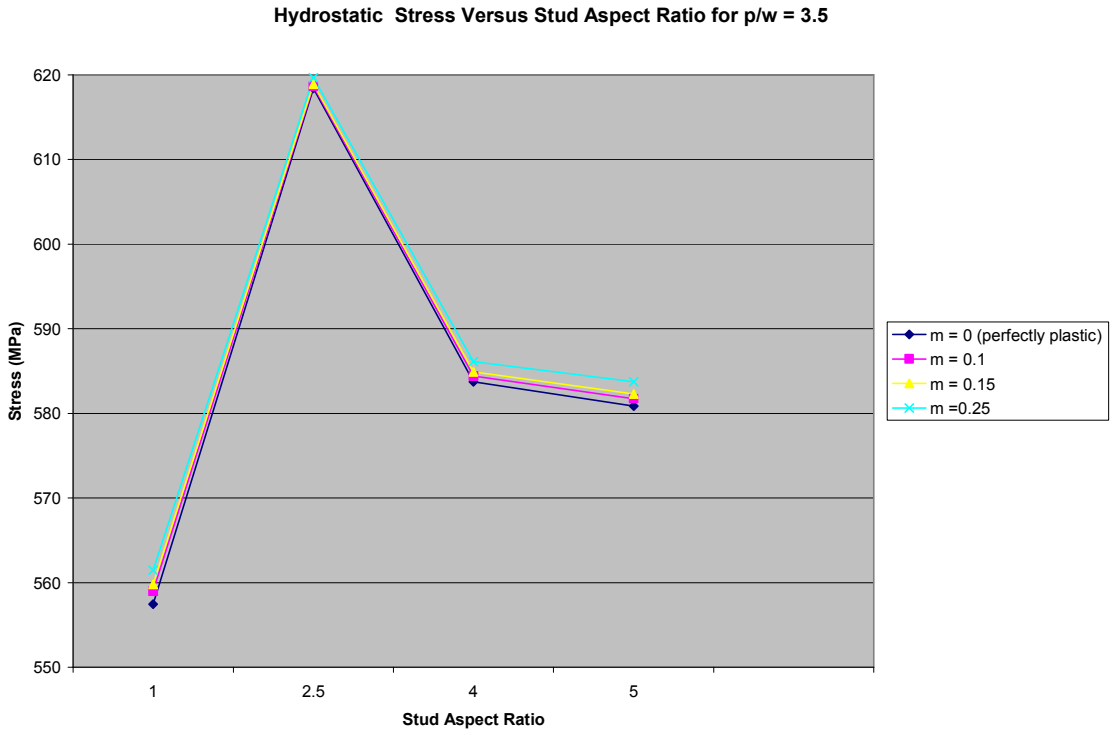

Figure 16- Hydro stress for p/w =3.5

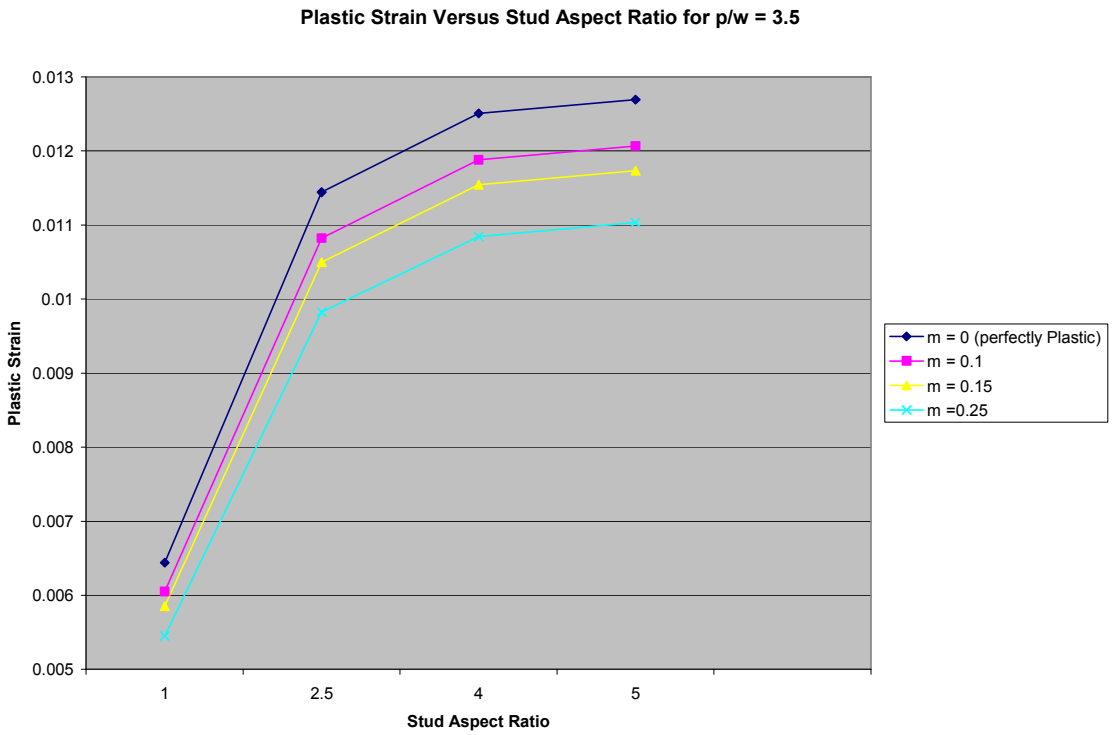

Figure 17- Pemag for p/w =3.5

m = 0 (perfectly plastic)					
h_s/w_s	***S11(MPa)***	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
1	561.4	625.01	527.725	571.378	0.00739
2.5	613.921	695.489	589.497	632.969	0.01239
4	589.845	679.19	573.355	614.13	0.01303
5	586.445	675.42	569.02	610.295	0.01322
m = 0.1					
h_s/w_s	***S11(MPa)***	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
1	561.669	633.81	524.455	573.311	0.006279
2.5	611.494	707.175	583.352	634.007	0.010688
4	586.5	691.86	567.595	615.318	0.011356
5	583.26	688.355	563.25	611.622	0.011551
m = 0.15					
h_s/w_s	***S11(MPa)***	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
1	561.82	638.375	522.785	574.327	0.006279
2.5	610.258	713.595	580.157	634.67	0.010688
4	584.755	698.805	564.58	616.047	0.011356
5	581.585	695.455	560.225	612.422	0.011551
m = 0.25					
h_s/w_s	***S11(MPa)***	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
1	562.055	647.7	519.415	576.39	0.006279
2.5	607.773	727.468	573.623	636.288	0.010688
4	581.15	713.86	558.38	617.797	0.011356
5	578.125	710.855	553.99	614.323	0.011551

Table 6 – Thermal stresses and plastic strain for p/w = 5

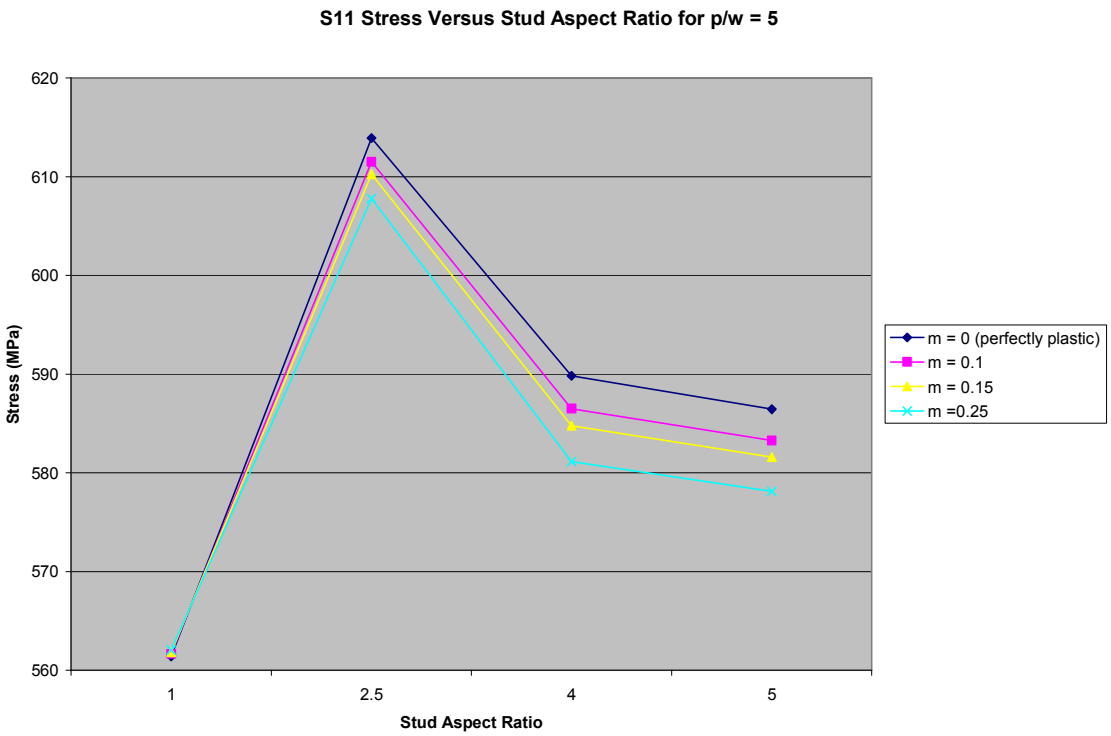

Figure 18- S11 stress for p/w =5

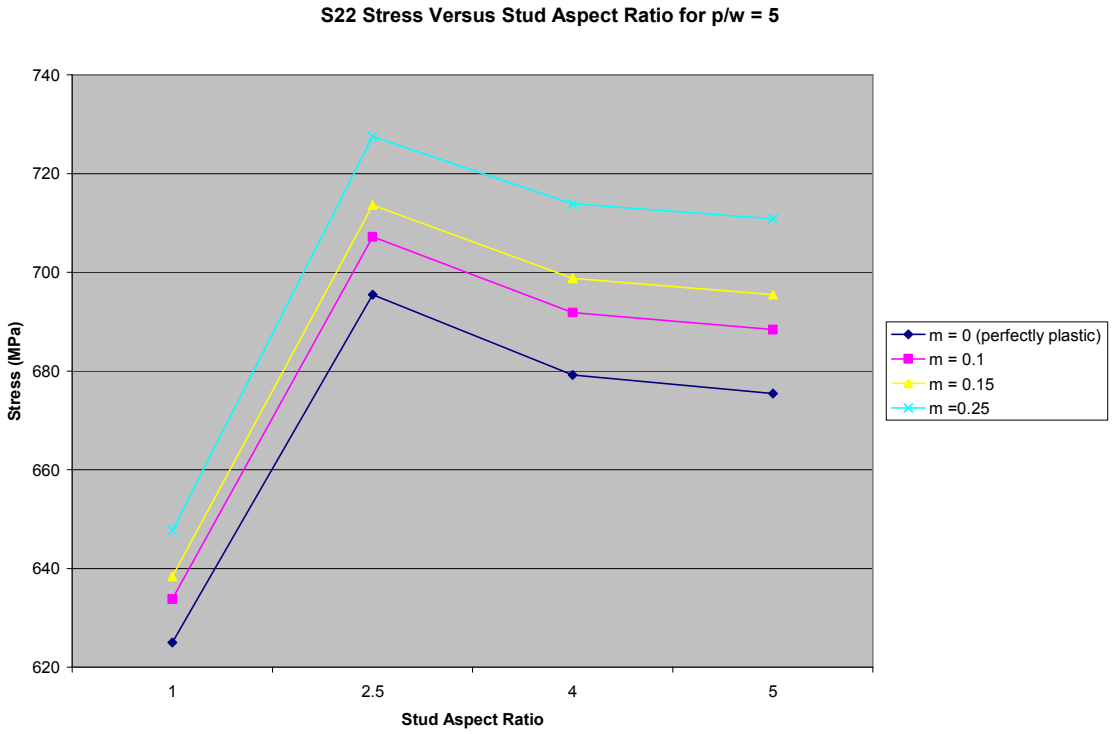

Figure 19- S22 stress for p/w =5

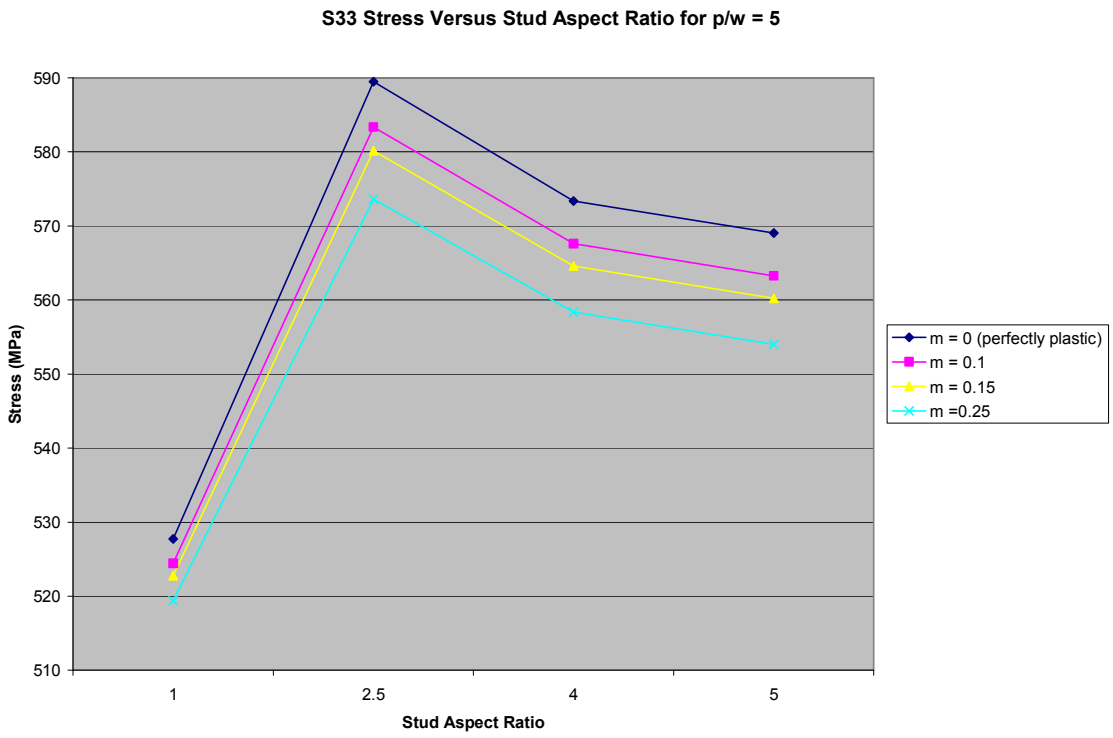

Figure 20- S33 stress for p/w =5

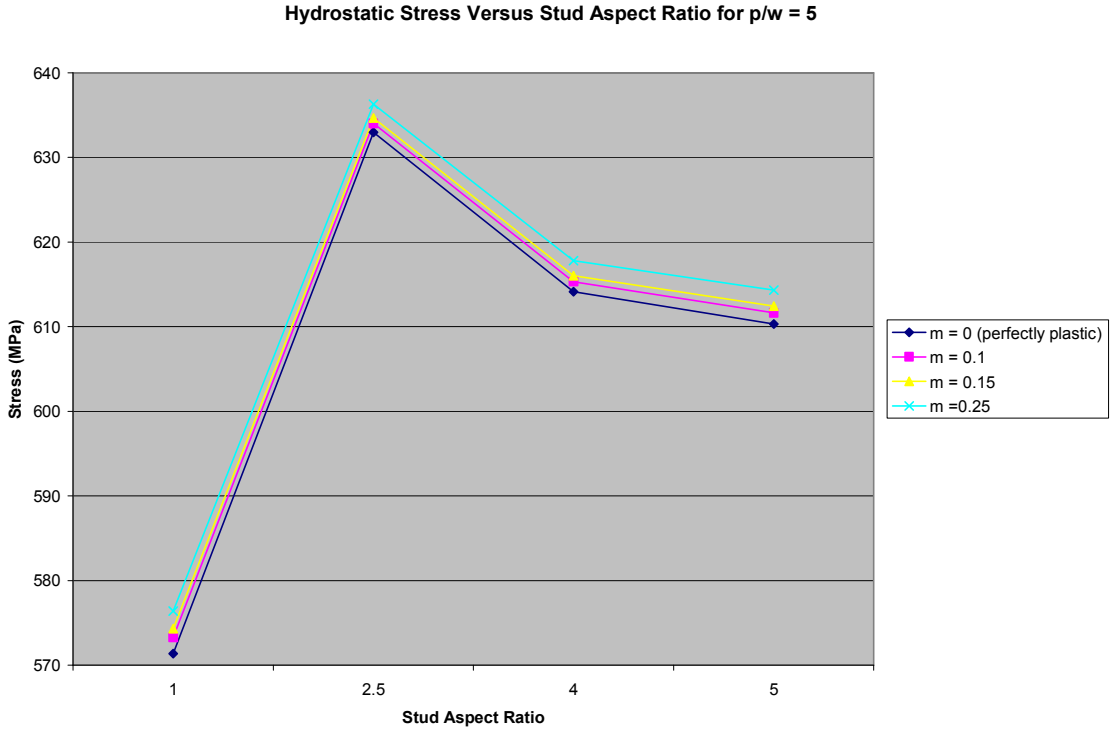

Figure 21- Hydro stress for p/w =5

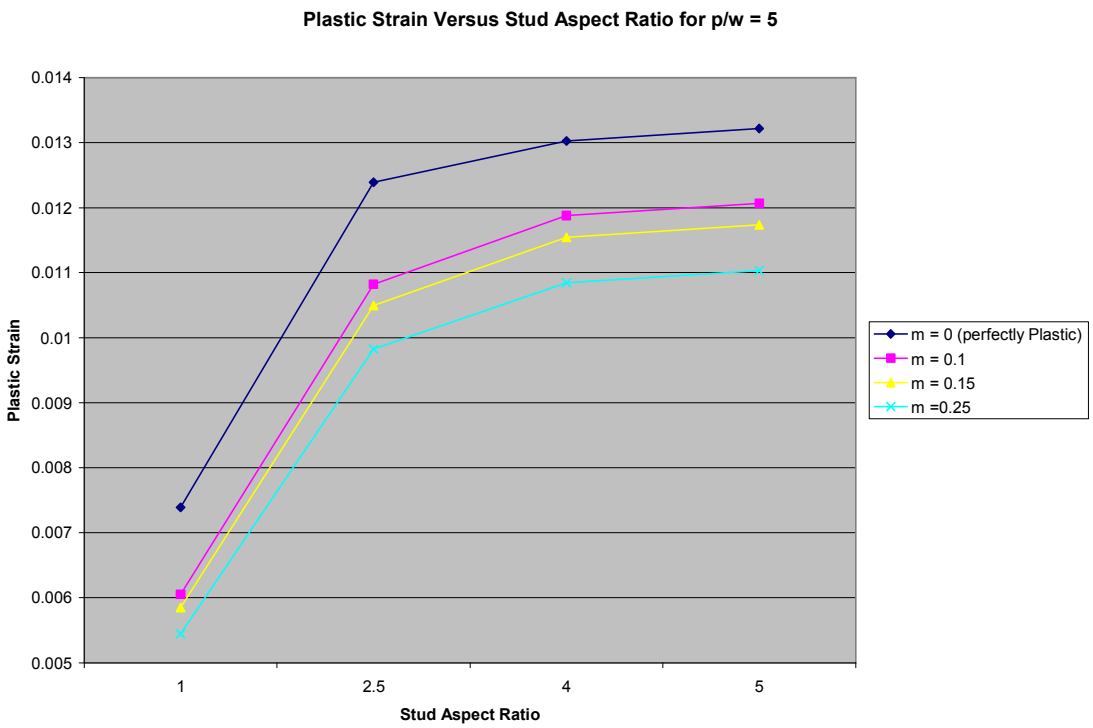

Figure 22- Pemag stress for p/w =5

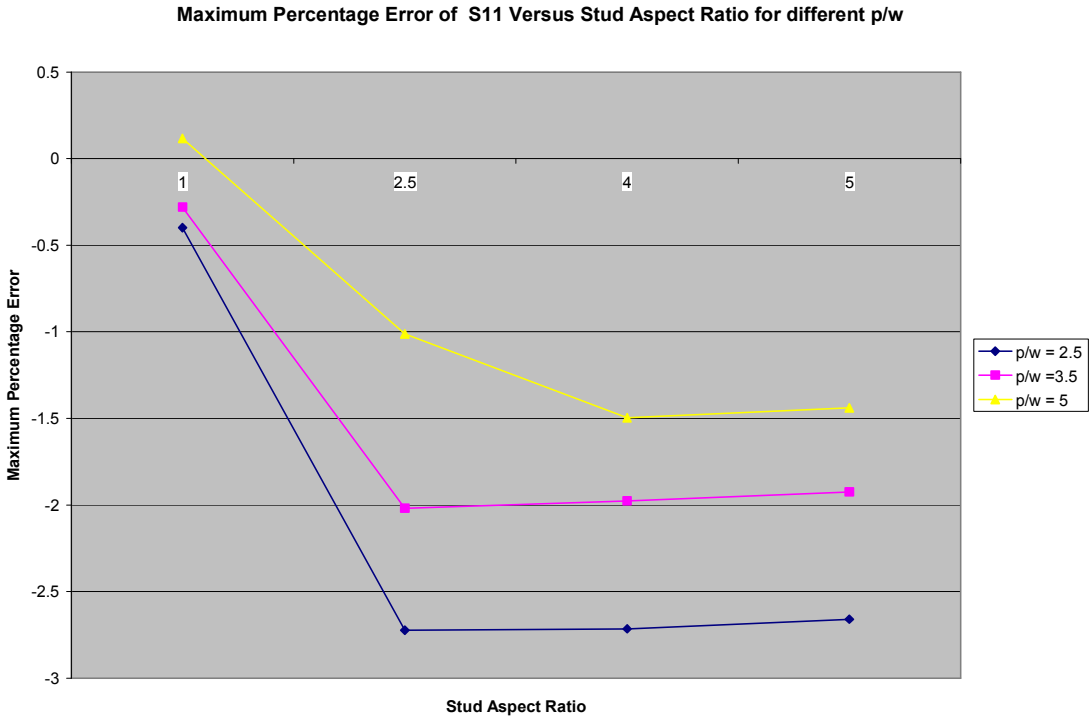

Figure 23- Maximum Error for S11 stress

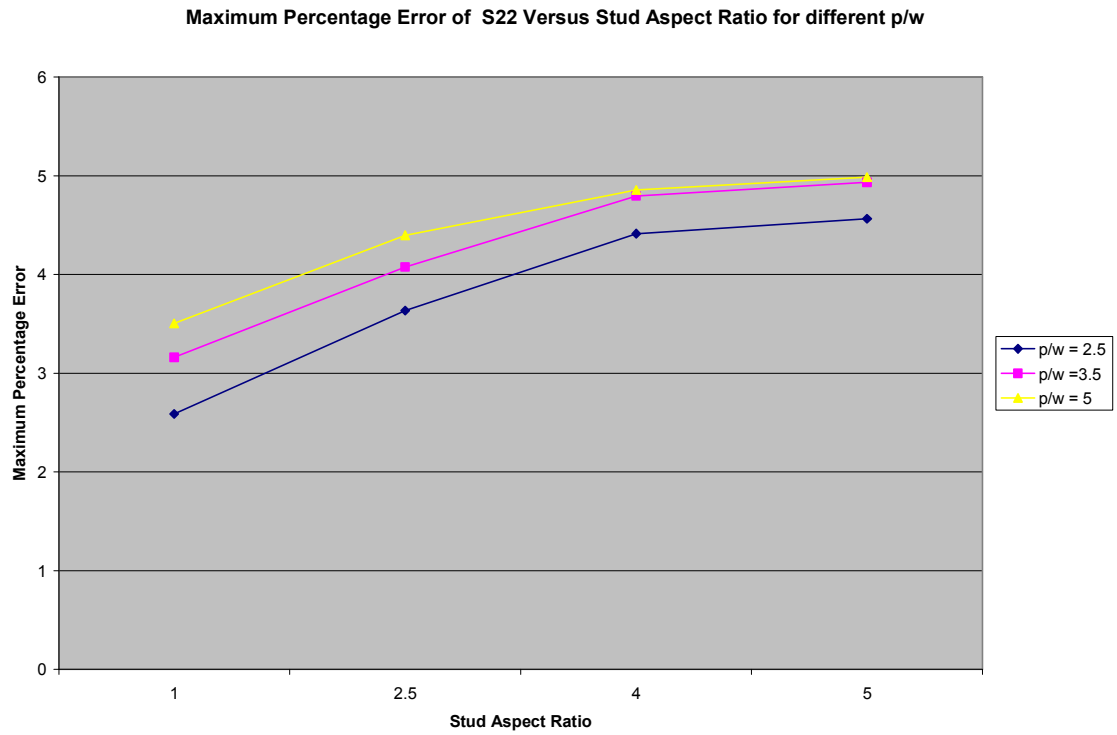

Figure 24- Maximum Error for S22 stress

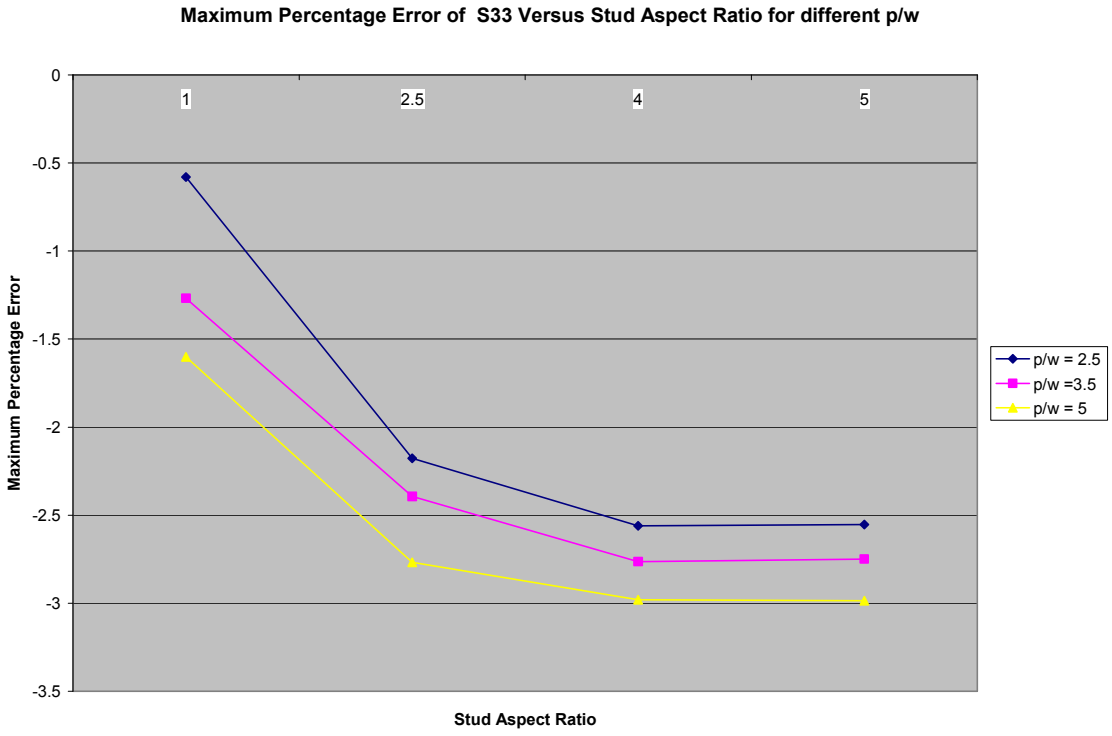

Figure 25- Maximum Error for S33 stress

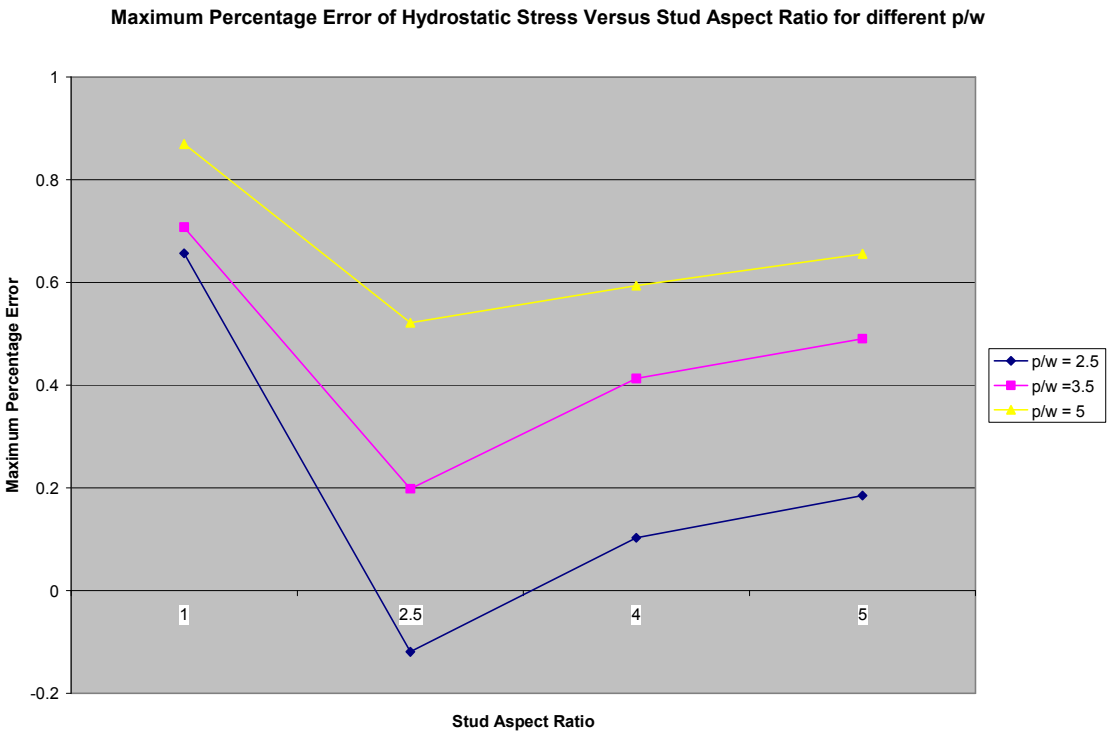

Figure 26- Maximum Error for Hydrostatic stress

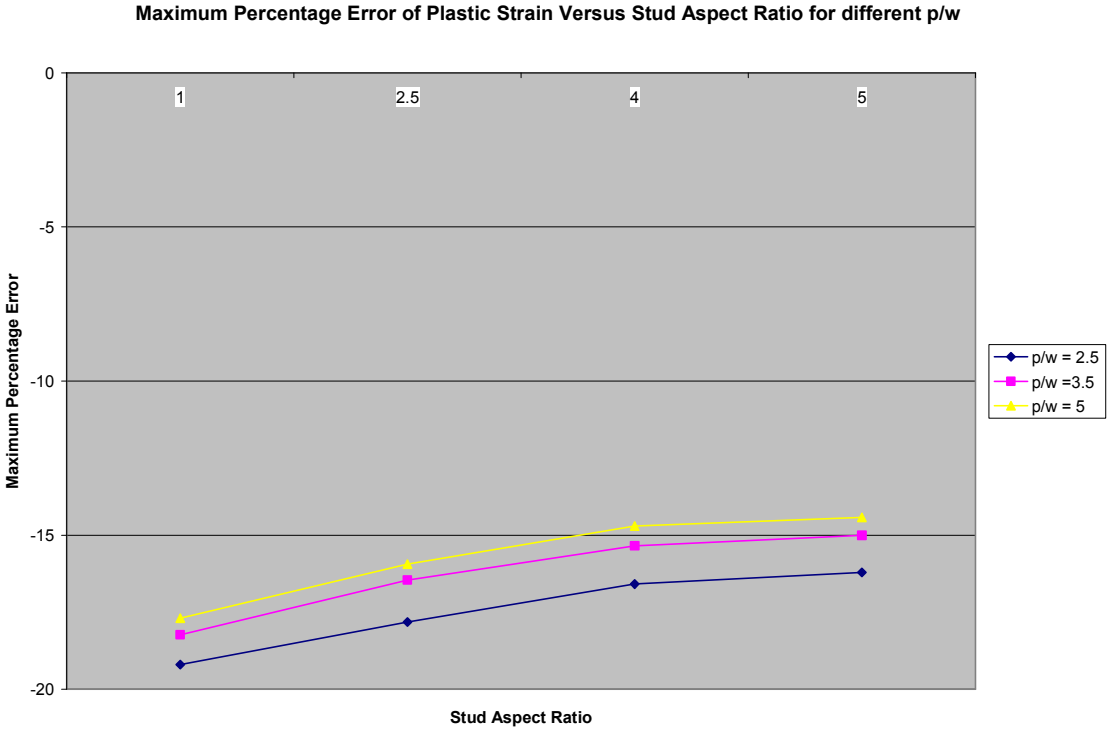

Figure 27- Maximum Error for Pemag

3.2 Effects of line spacing ratio on thermal stresses and plastic strain for aluminum stud/via

The effect of line spacing ratio p/w on thermal stresses and plastic strain of the aluminum stud was determined in this section. Using tables and graphs used in the previous section but considering the case of m= 0(that is perfectly plastic) the following graphs were obtained. Similar trend is also obtainable for m = 0.1, 0.15 and 0.25

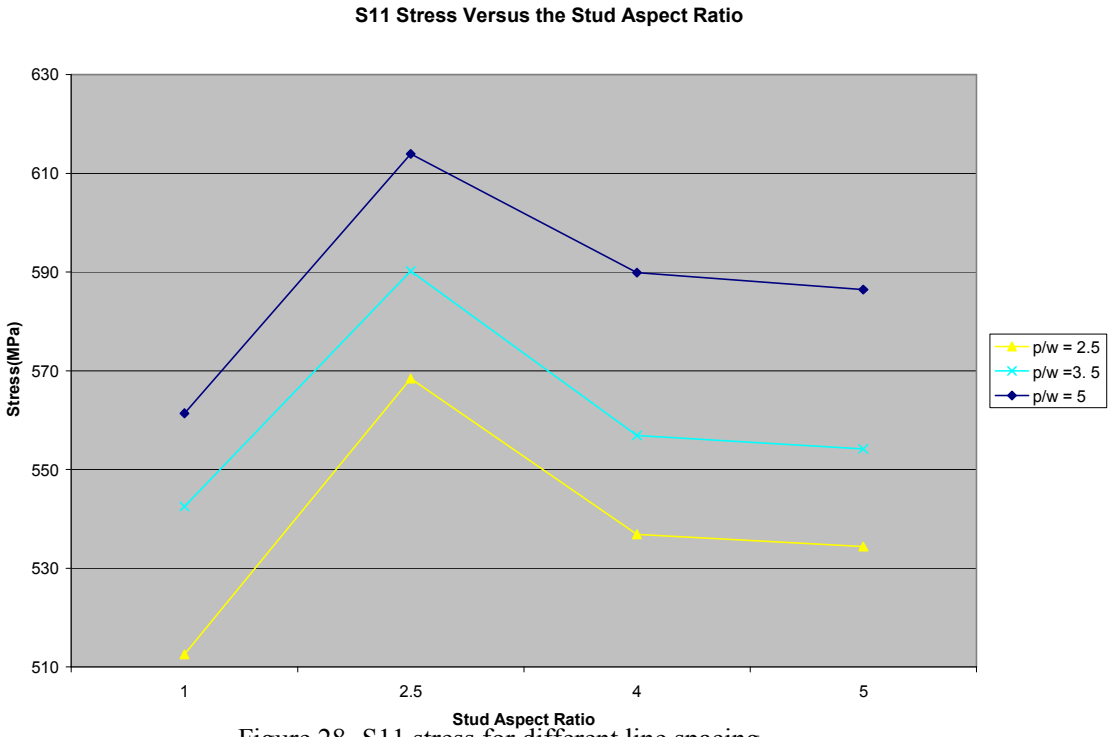

Figure 28- S11 stress for different line spacing

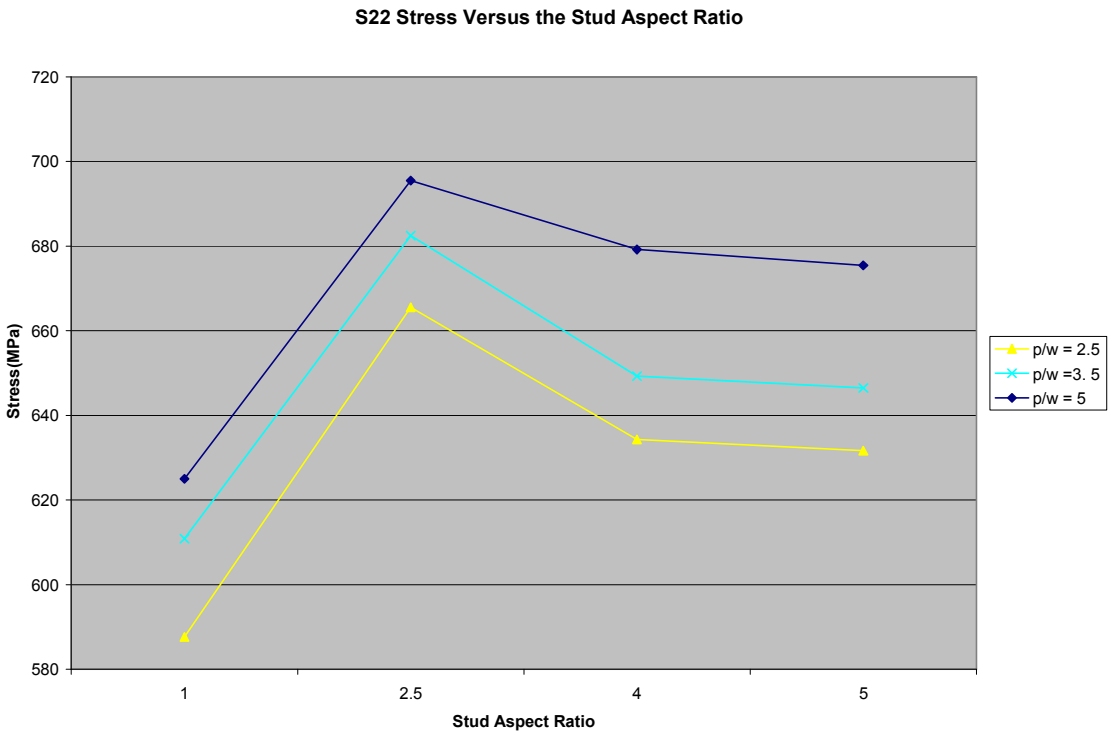

Figure 29- S22 stress for different line spacing

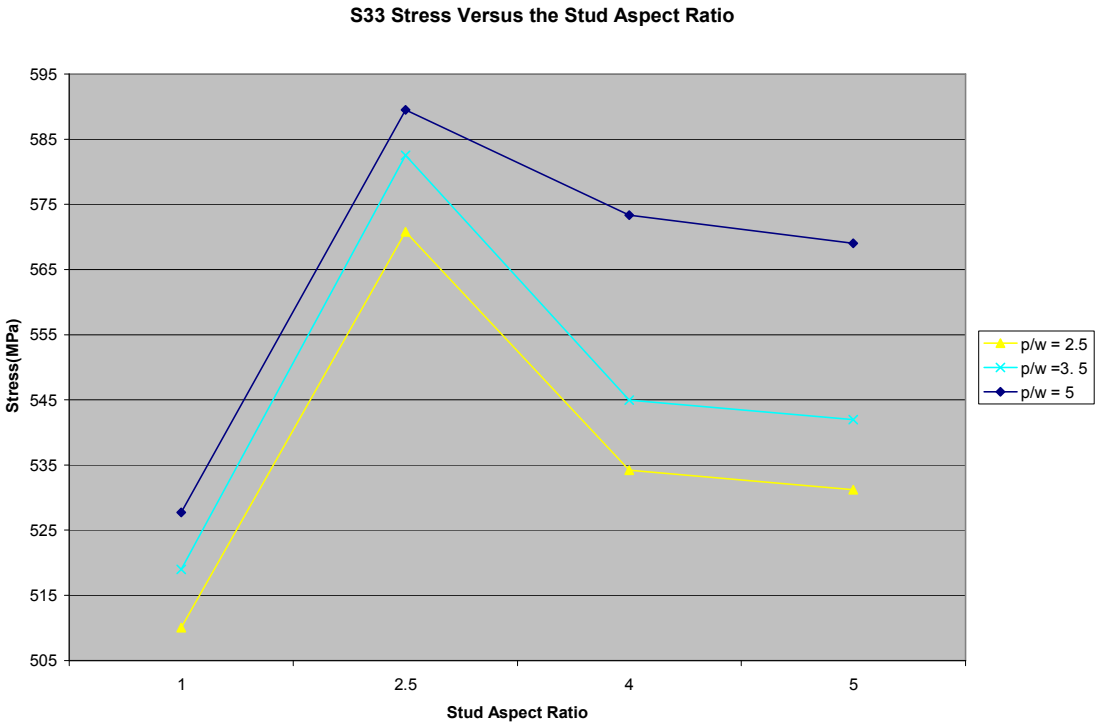

Figure 30- S33 stress for different line spacing

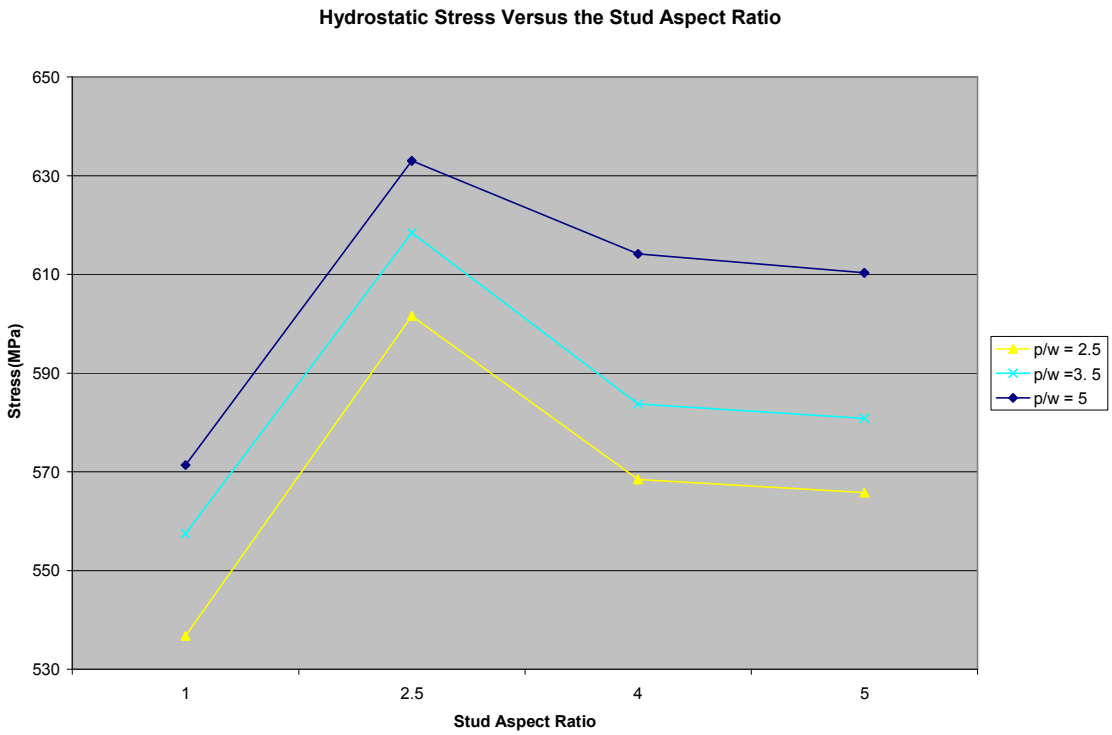

Figure 31- Hydro stress for different line spacing

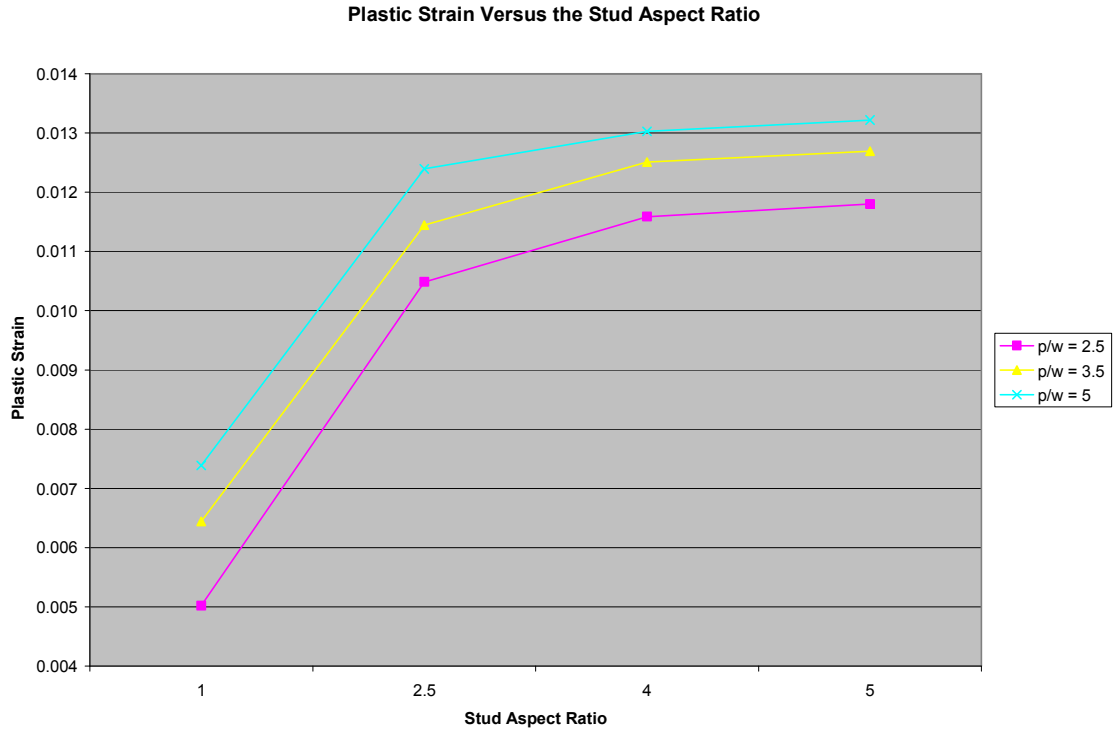

Figure 32- Pemag for different line spacing

3.4 Discussion of results for sections 3.1 and 3.2

- In order to achieve higher integration by placing the interconnects closer (that is reducing line spacing ratio p/w) there will be reduction in the stresses and plastic strain in the studs (Figures 28 –32) at the expense of increase in stresses in the interconnects
- The stresses exhibited a peak value at a stud aspect ratio of 2.5 for the range of aspect ratio considered.Consequently the propensity of voiding is increased as the stud aspect ratio approaches 2.5 but reduces for increasing stud aspect ratio at the expense of increase in plastic deformation. The plastic deformation is a mechanism for stress relaxation. Similar trend for aluminum interconnects was observed in previous studies [5] with maximum stresses having a peak value at line aspect ratio between 1.5 to 1.75
- The magnitude of tensile hydrostatic stress component which is an indication of propensity of void formation exhibited little dependence on the hardening exponent m (Figures 11,16 and 21). The maximum absolute percentage error was between 0.2% to 0.9% (Figure 43). The assumption of perfectly plastic is justifiable for prediction of the hydrostatic stress component in aluminum studs. The error increases for widely spaced interconnects consequently the assumption of perfectly plastic will give the best estimate of the hydrostatic stress in aluminum studs for closely spaced interconnects.

- The individual normal stress components that are responsible for the anisotropic growth of void showed moderate dependence on the hardening exponent m. The maximum absolute percentage error within the range of 0.4% to 5% (Figures 24-25). The perfectly plastic assumption gives a good estimate of the individual stress components for closely spaced interconnects and reducing stud aspect ratio except for one of the stresses (S11) that gave a good estimate for increasing interconnect spacing. The stress in the direction of stud height (S22) had the maximum value indicating that once voids are formed, the preferred direction of void growth will be in the height direction which was in agreement with previous studies on studs [8-9]
- The magnitude of plastic strain exhibited dependence on the hardening exponent m (Figures 12,17,22) .The maximum absolute percentage error in the range between 14% to19%.The error increases for closely spaced interconnects and increasing stud aspect ratio (Figure 27).If plastic strain is the primary variable of concern the perfectly plastic assumption is not a good estimate of plastic strain in aluminum studs

3.4 Effects of different materials on thermal induced stress and plastic strain in studs

This section looks at the effects of changes in material choice for dielectric, stud and interconnects on the induced thermal stresses and plastic strain. As mentioned earlier in previous section, the trend in microelectronic circuitry is to gradually replace SiO_2 with low k dielectrics and to replace Al_3 with Cu for both metal interconnects and stud. This trend will have an effect on the thermo-mechanical reliability of studs.

In this section, eight models were considered with each model having the following material choices as shown in Table 7. The model considered was at the 100nm design node for a DRAM according to the National Technology Roadmap for Semiconductors [23]. The summary of number of elements and geometric parameters used is shown on Table 8. The interconnect with Al_3 and Cu had a TiN diffusion barrier layer thickness of 11nm while W interconnect had no diffusion barrier layer.

Model	Material		
	Interconnect	Via/Contact	Dielectric
1	Al_3	Al_3	SiO_2
2	Al_3	W	SiO_2
3	W	W	SiO_2
4	Cu	Cu	SiO_2
5	Al_3	Al_3	SiLK
6	Al_3	W	SiLK
7	W	W	SiLK
8	Cu	Cu	SiLK

Table 7- Listing of material choices for models 1 to 8

Number of Elements	H(nm)	L(nm)	h(nm)	w(nm)	h_s(nm)	w_s(nm)	p(nm)
12150	4386	21930	240	100	900	100	

Table 8 - Summary of parameters used for sections 3.5 and 3.6

Model 1					
	S11(MPa)	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
C	555.156	662.282	610.088	544.462	0.00571
S1	560.947	664.892	605.574	610.471	0.0051
S2	558.967	662.432	600.804	607.401	0.00494
Model 2					
	S11(MPa)	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
C	-8.2193	290.287	94.559	125.542	0
S1	-14.191	272.41	28.2056	95.4747	0
S2	-18.878	244.069	6.15019	77.1138	0
Model 3					
	S11(MPa)	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
C	50.8815	317.008	146.778	171.556	0
S1	58.5301	303.942	128.542	163.671	0
S2	58.663	289.525	124.48	157.556	0
Model 4					
	S11(MPa)	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
C	330.611	533.201	431.173	431.662	0.00218
S1	344.814	542.015	424.395	437.075	0.00187
S2	344.194	536.908	418.38	433.161	0.00179
Model 5					
	S11(MPa)	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
C	2.97907	-84.951	22.1898	-19.927	0.03187
S1	-2.7921	-88.664	20.12	-23.779	0.03185
S2	-4.8163	-88.925	20.4723	-24.423	0.03048
Model 6					
	S11(MPa)	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
C	-69.908	-2965.6	45.239	-996.75	0
S1	-112.13	-2537.8	103.821	-848.69	0
S2	-161.12	-1961.1	80.0253	-680.74	0
Model 7					
	S11(MPa)	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
C	-48.308	-5235.6	-46.496	-1776.8	0
S1	-120.81	-4925.5	8.02855	-1679.4	0
S2	-162.99	-3851.3	34.2752	-1326.7	0
Model 8					
	S11(MPa)	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
C	-17.323	-882.22	12.7256	-295.6	0.02026
S1	-43.659	-867.74	16.5037	-298.3	0.0195
S2	-44.865	-769.33	30.3571	-261.28	0.01723

Table 9-Thermal stress and plastic strain for models 1 to 8

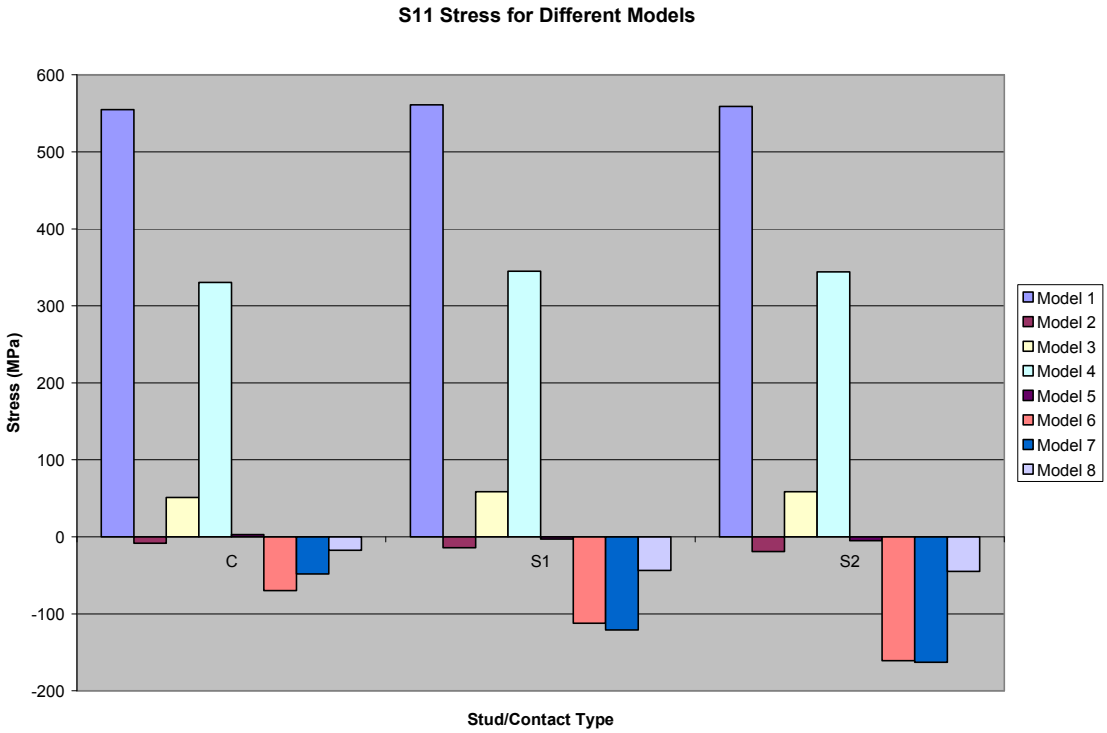

Figure 33- S11 for different Models

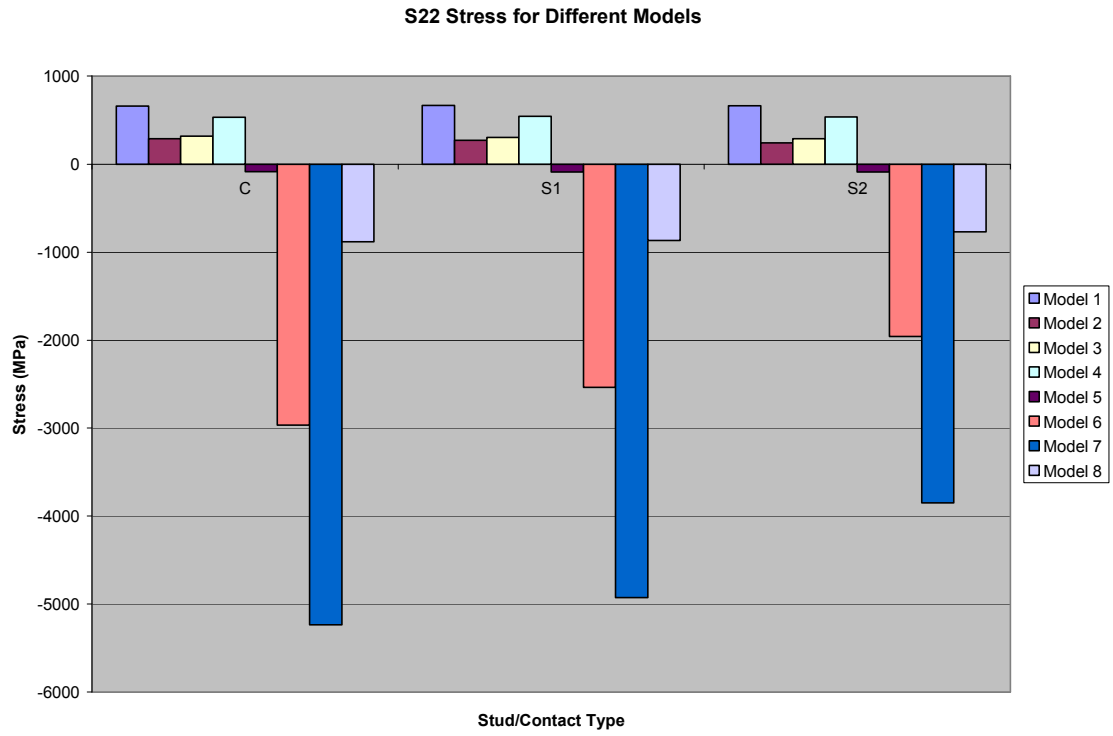

Figure 34- S22 for different Models

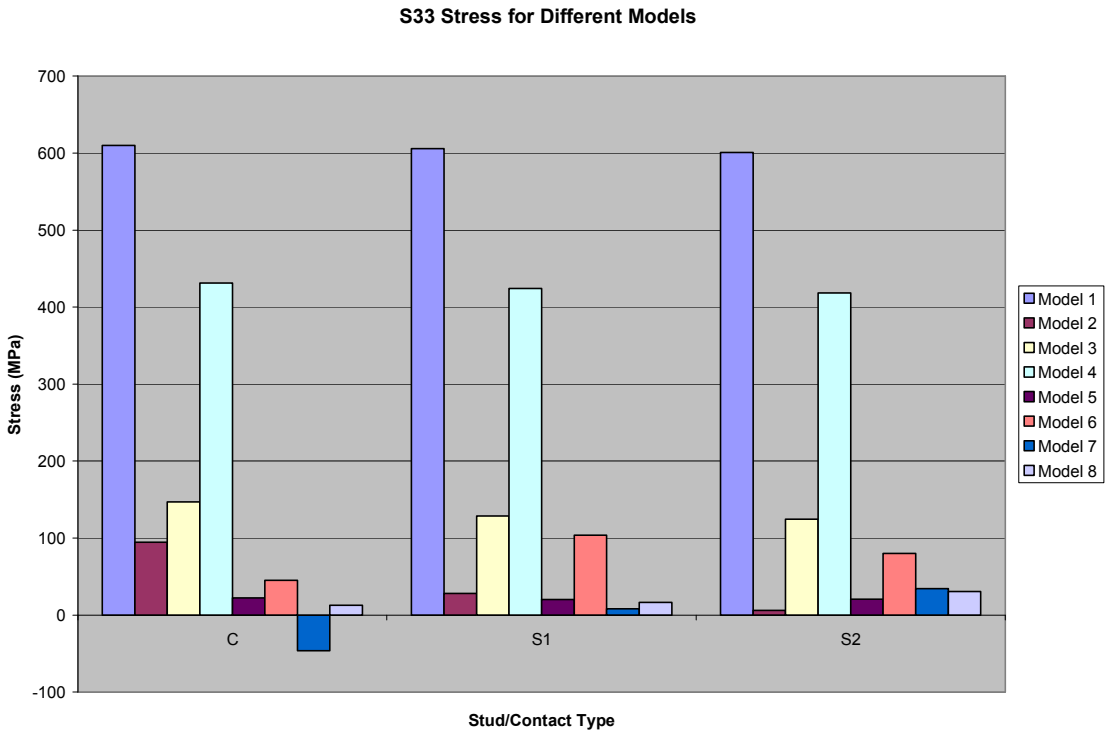

Figure 35- S33 for different Models

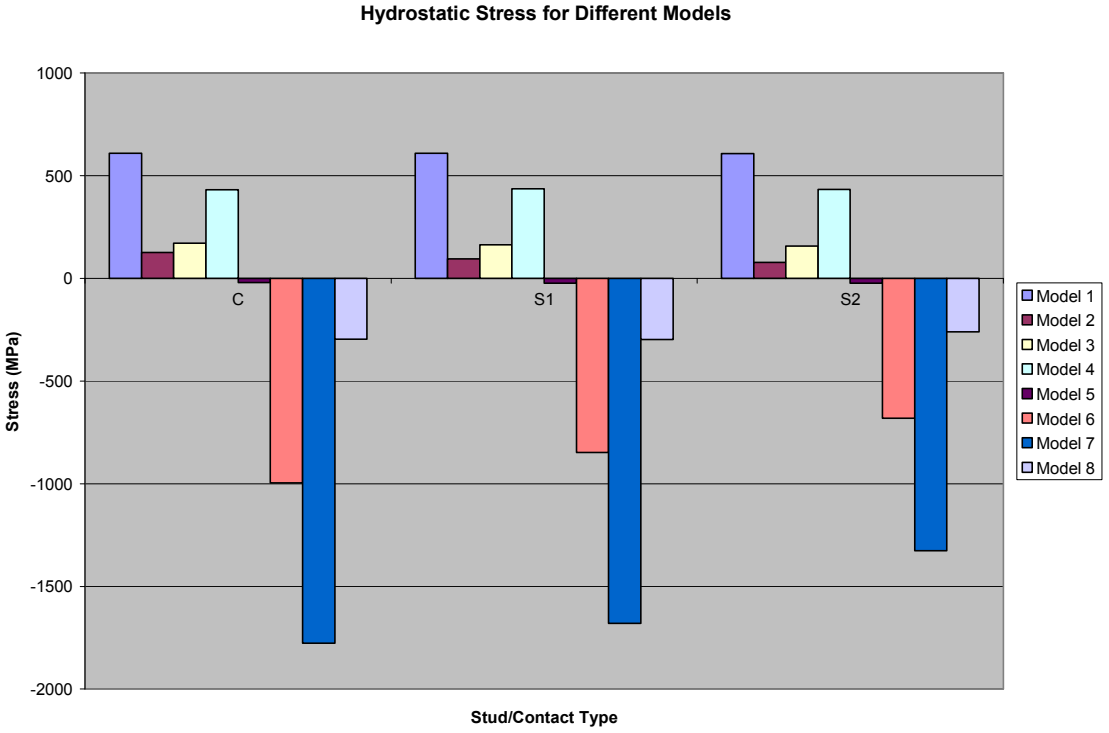

Figure 36- Hydro for different Models

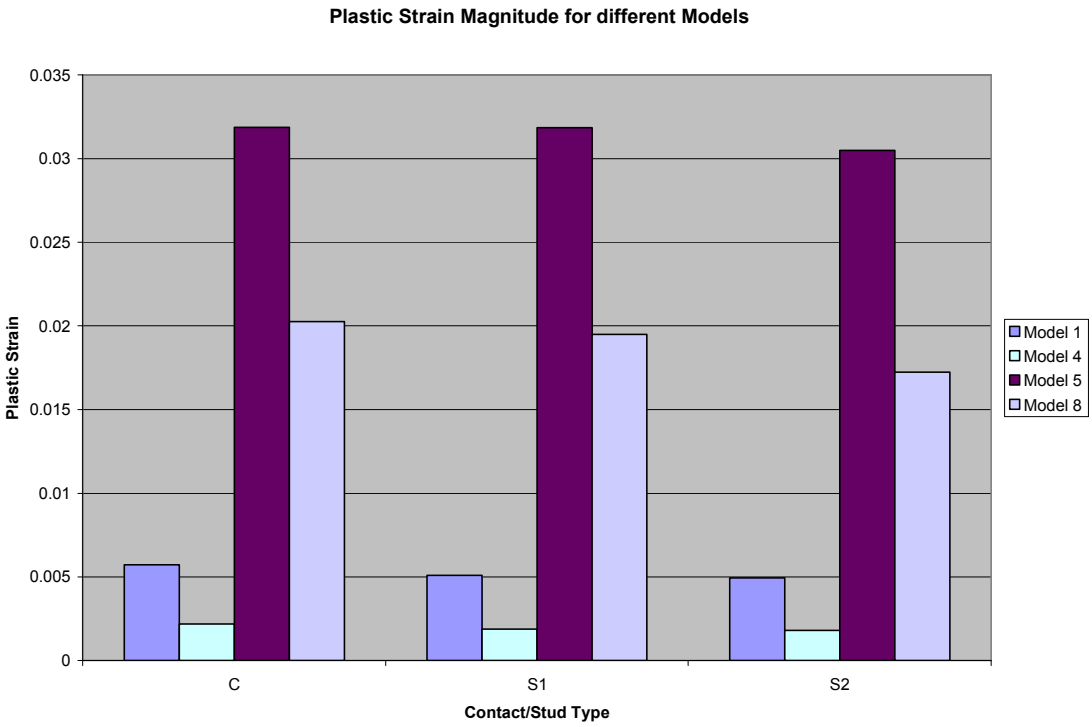

Figure 37- Pemag for different Models

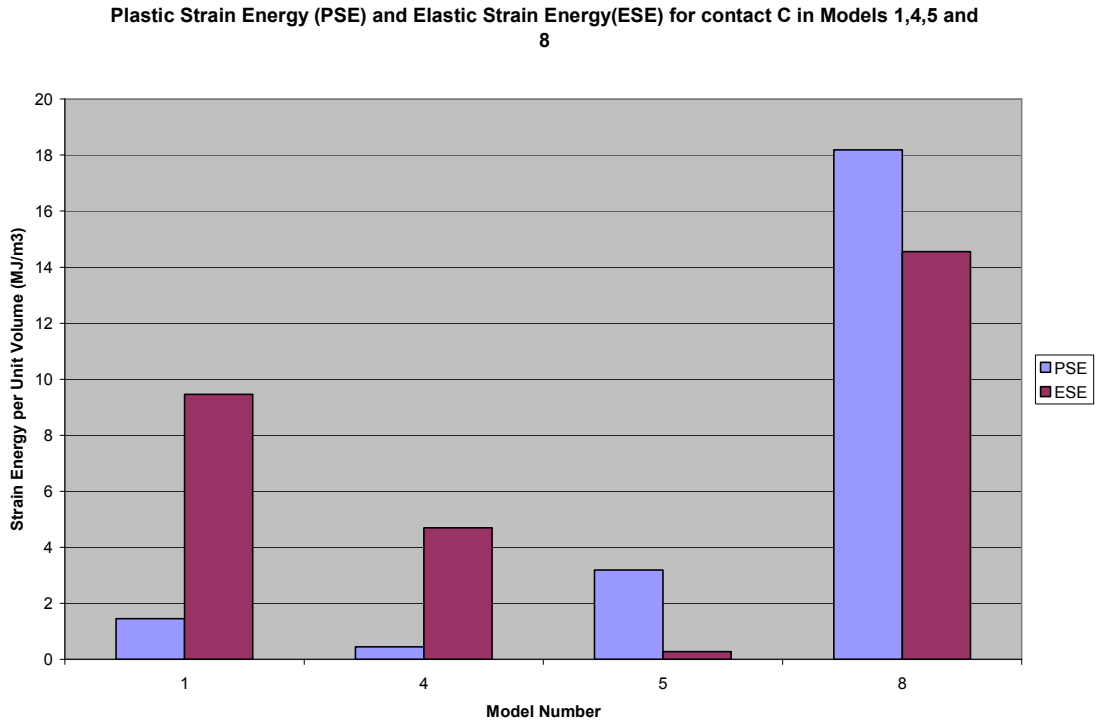

Figure 38- PSE and ESE of Contact C for Models 1,4,5,8

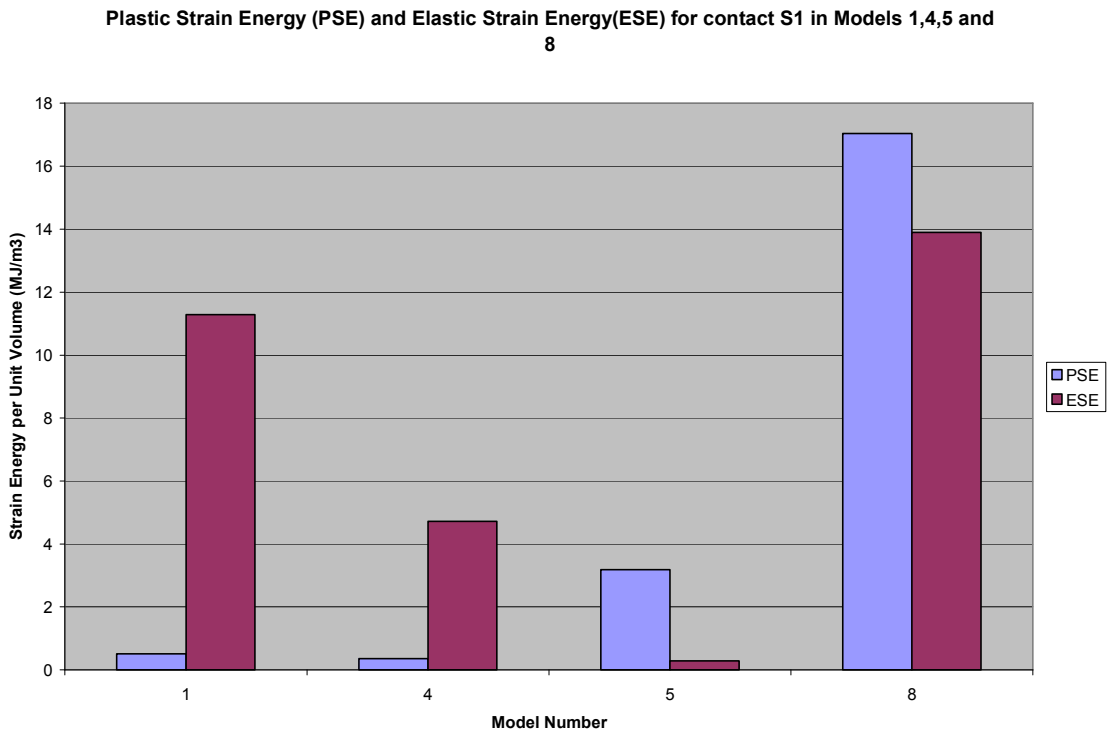

Figure 39- PSE and ESE of stud S1 for Models 1,4,5,8

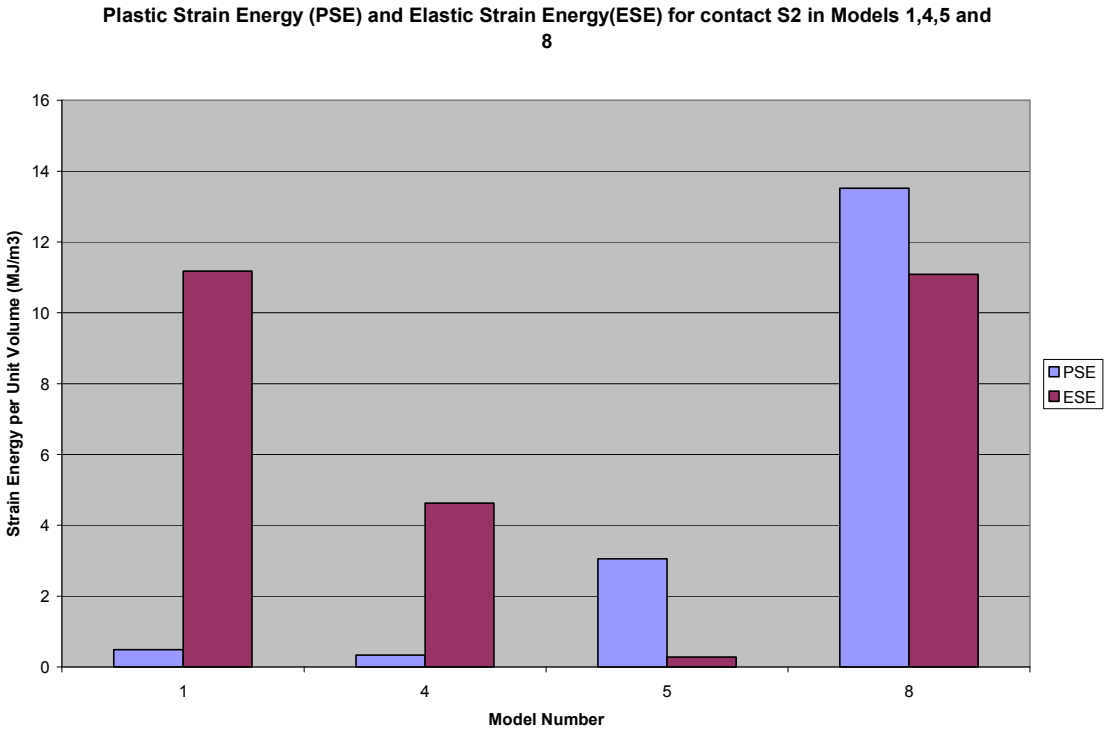

Figure 40- PSE and ESE of stud S1 for Models 1,4,5,8

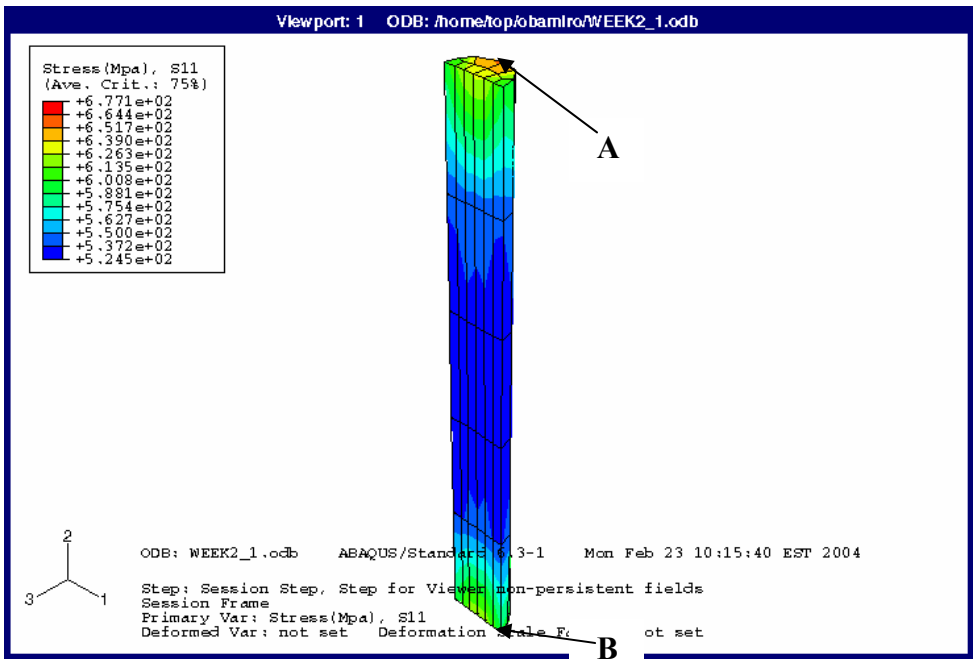

Figure 41a- S11 contour plot for front view of S1 of Model 1

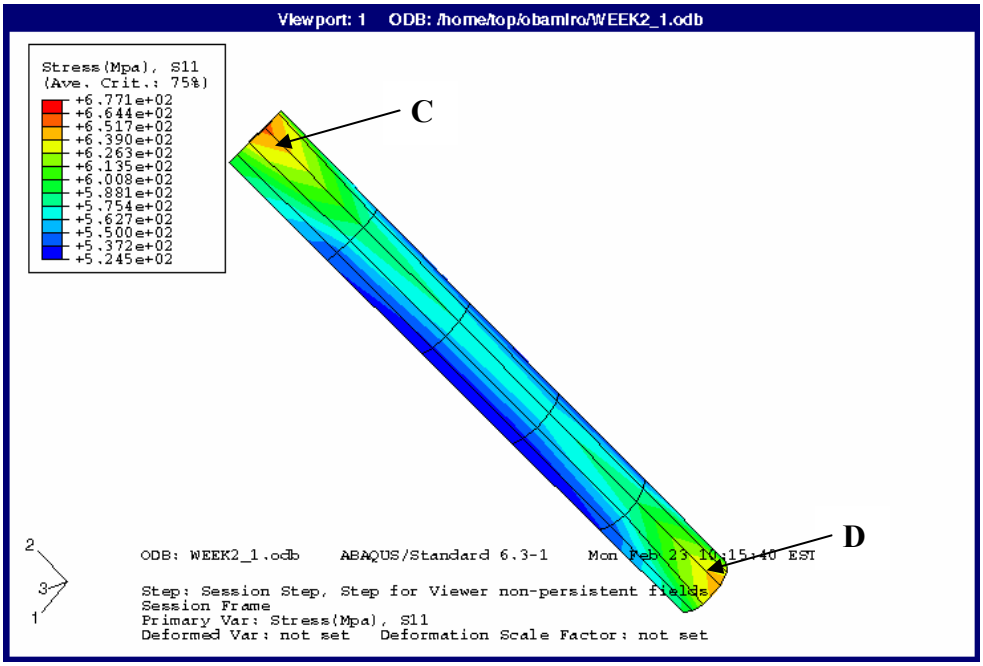

Figure 41b- S11 contour plot for back view of S1 of Model 1

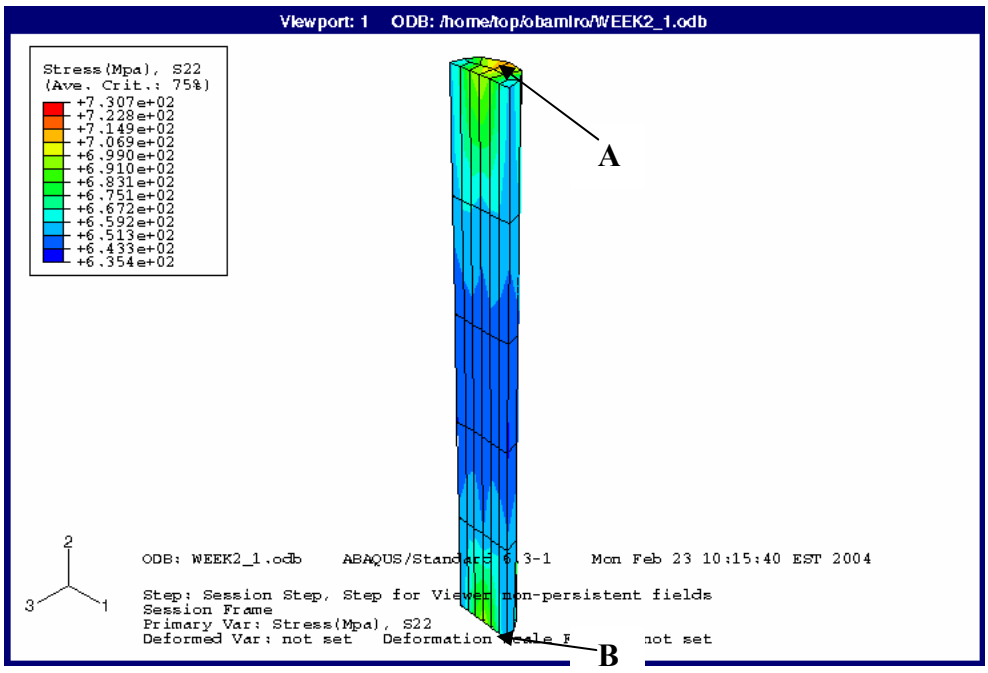

Figure 42a – S22 contour plot for front view of S1 for Model 1

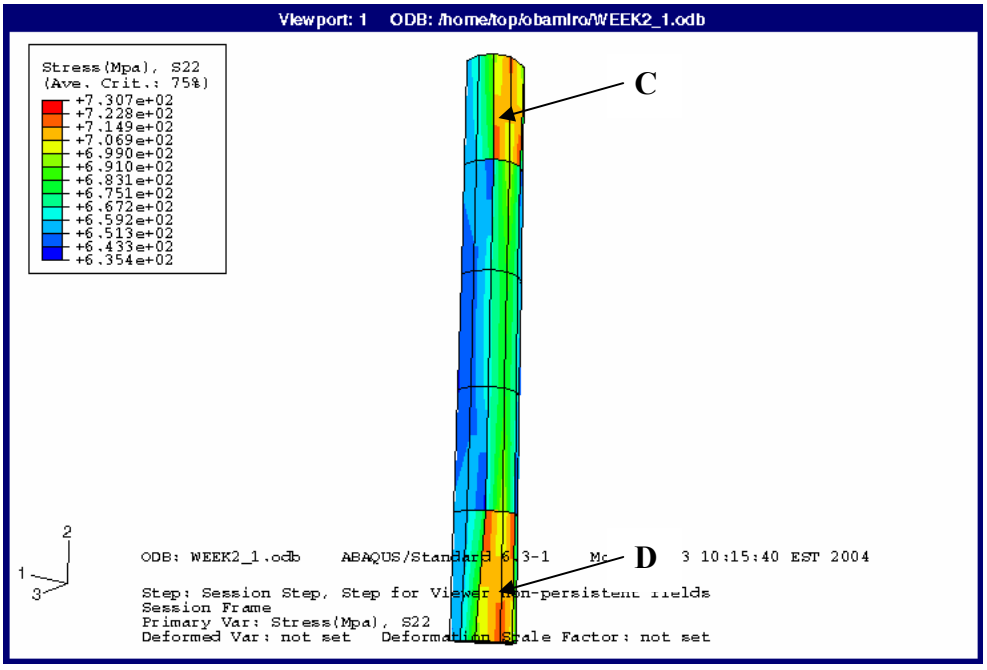

Figure 42b – S22 contour plot for back view of S1 for Model 1

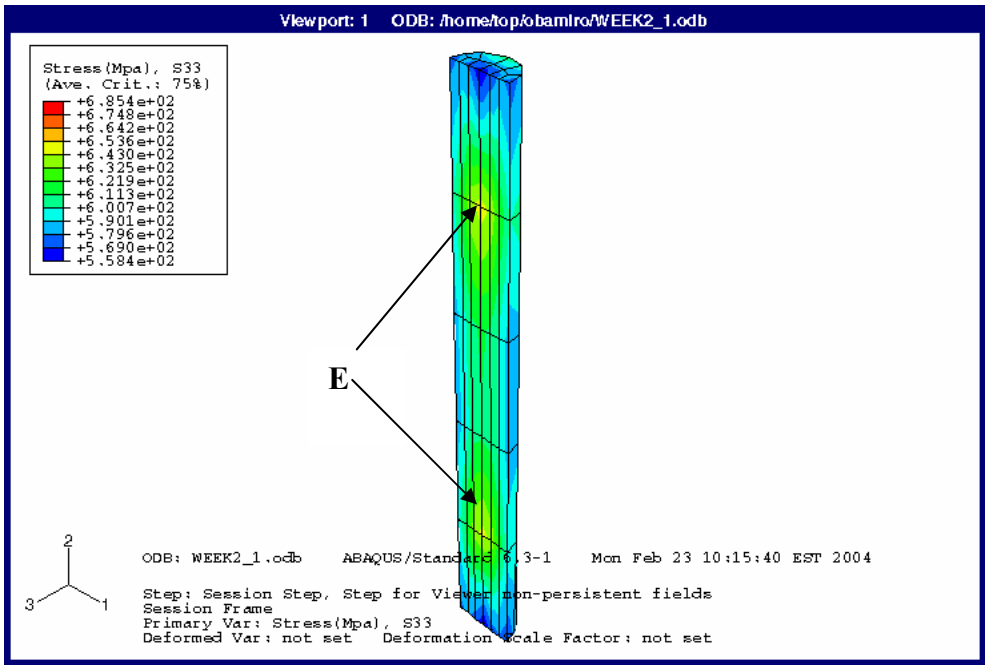

Figure 43a – S33 contour plot for front view of S1 for Model 1

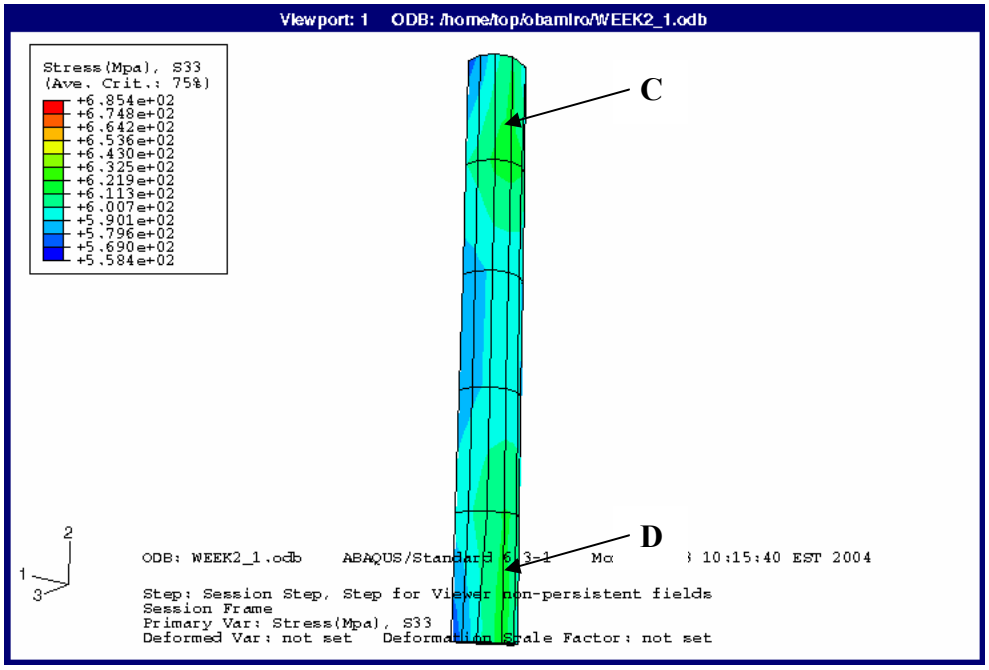

Figure 43b – S33 contour plot for back view of S1 for Model 1

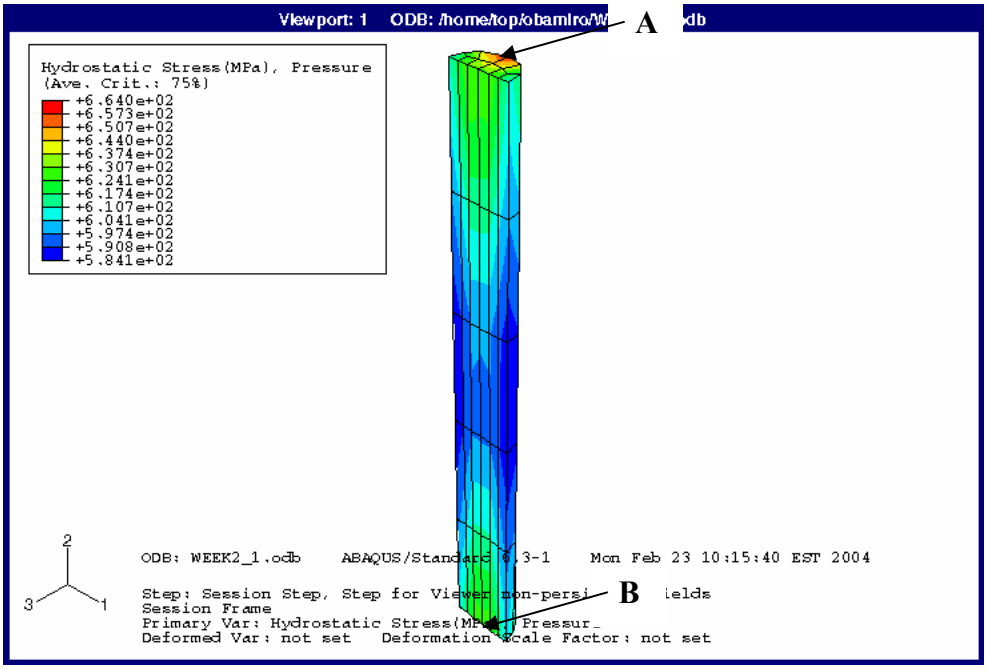

Figure 44a – Hydro contour plot for front view of S1 for Model 1

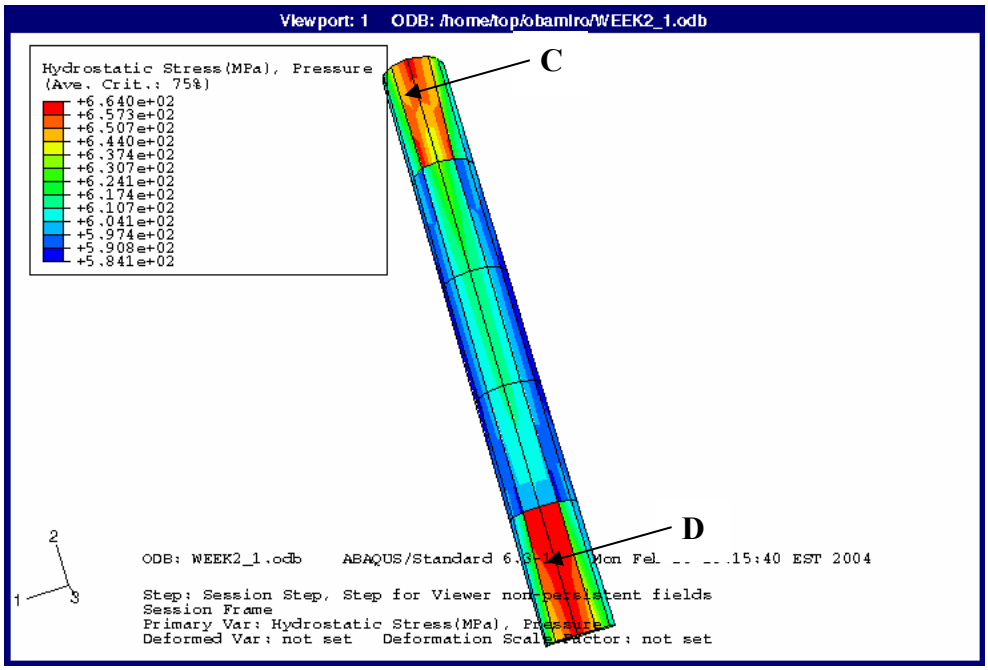

Figure 44b – Hydro contour plot for back view of S1 for Model 1

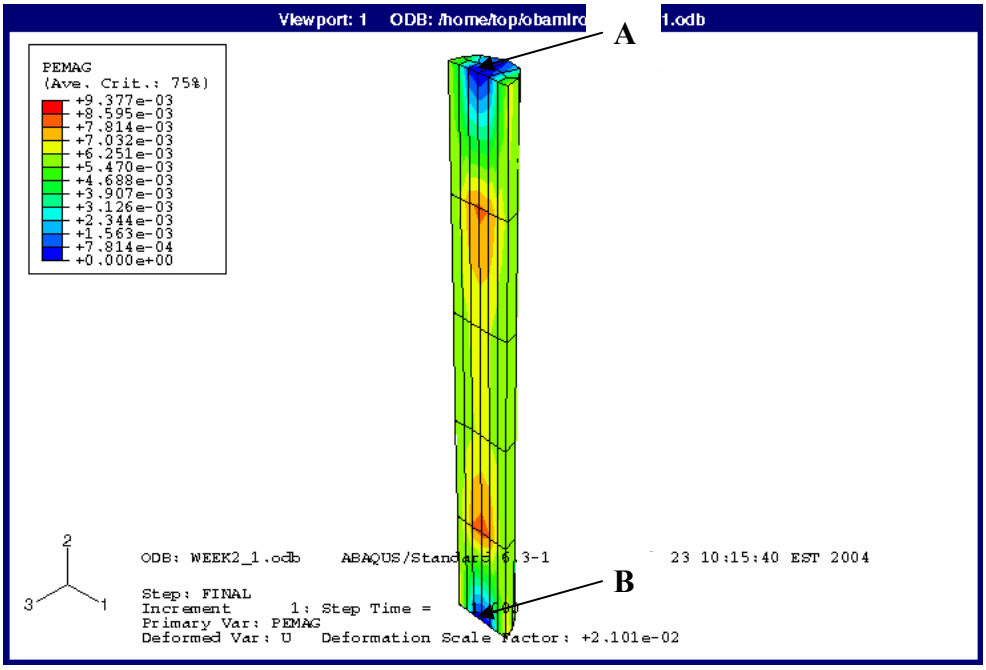

Figure 45a – Pemag contour plot for front view of S1 for Model 1

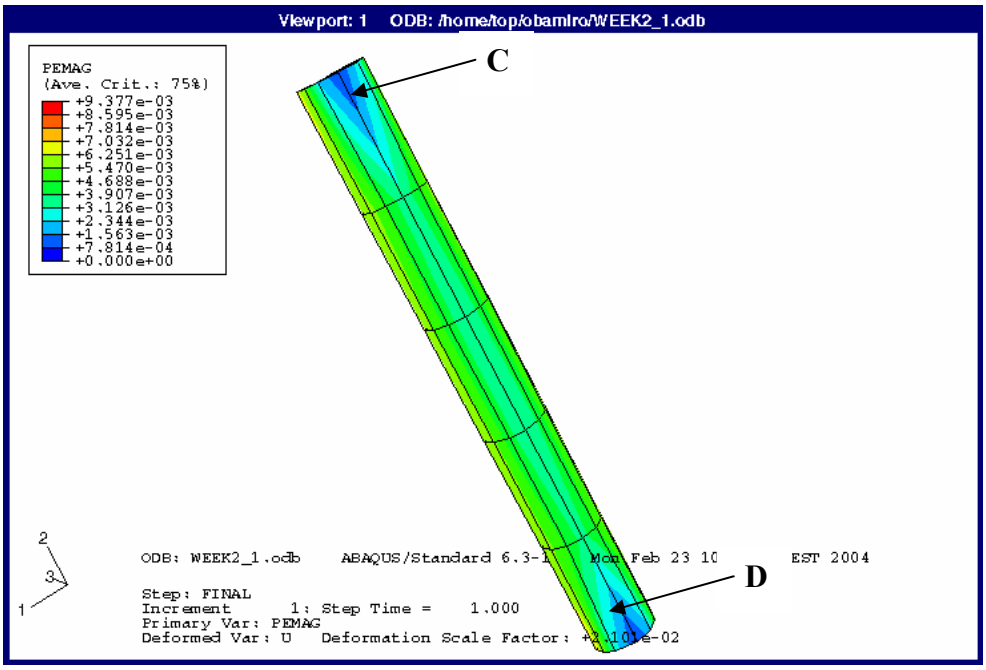

Figure 45b – Pemag contour plot for back view of S1 for Model 1

3.5 Diffusion barrier effect on thermal induced stress and plastic strain in studs

The effects of TiN diffusion layer on the stresses and plastic strain in studs was determined in this section. Diffusion layers are used to prevent diffusion of Cu or Al_3 atoms from diffusing into the dielectric or silicon substrate. In previous research [8-9], the effects of the diffusion layer is ignored. A TiN thickness of 11nm was used with the studs in models 1, 4, 5 and 8 to become models 9,10, 11 and 12.

Model 9					
	S11(MPa)	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
C	706.599	815.735	754.949	759.094	0.00349
S1	703.049	810.091	743.822	752.321	0.0031
S2	700.885	807.656	741.393	749.978	0.00307
Model 10					
	S11(MPa)	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
C	485.429	683.201	570.304	579.645	0.0016
S1	488.407	674.108	556.772	573.096	0.00142
S2	486.344	670.197	553.729	570.09	0.00139
Model 11					
	S11(MPa)	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
C	461.811	373.742	478.423	437.992	0.00666
S1	486.277	405.44	511.196	467.638	0.01103
S2	501.915	431.561	537.09	490.189	0.00775
Model 12					
	S11(MPa)	***S22(MPa)***	***S33(MPa)***	***Hydro(MPa)***	***Pemag***
C	160.327	-460.41	199.382	-33.566	0.01097
S1	152.357	-395.03	221.133	-7.1787	0.00993
S2	174.611	-241.29	255.815	63.044	0.00767

Table 10 – Diffusion barrier effect on stresses and plastic strain

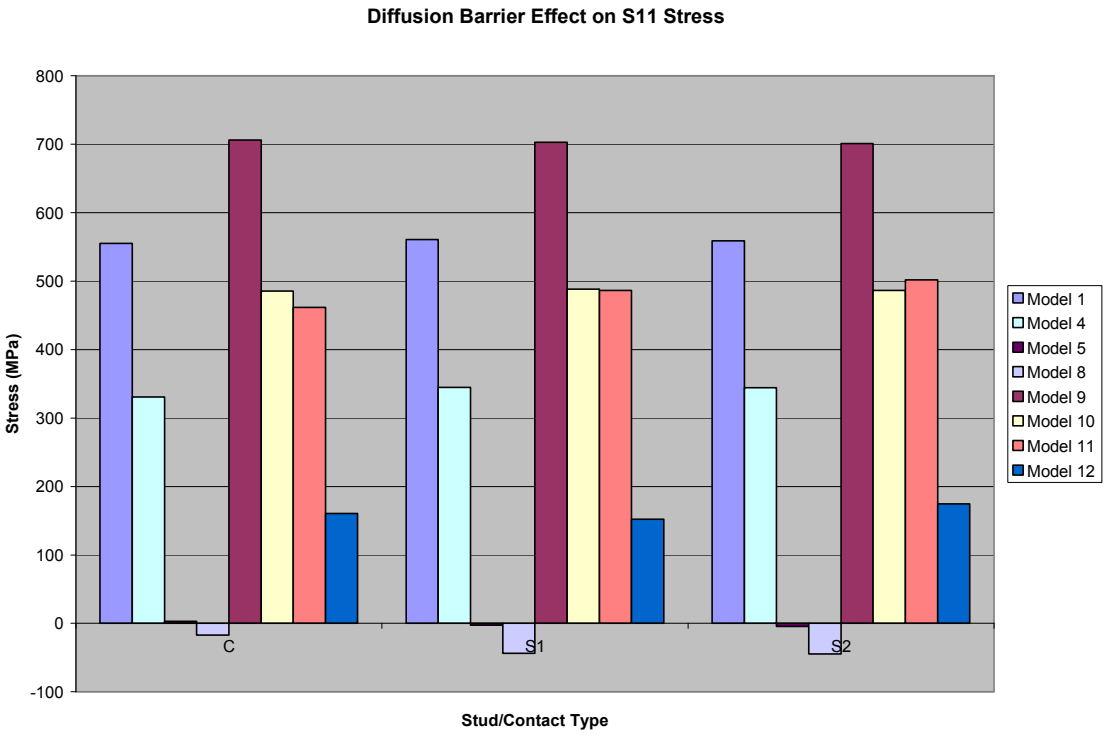

Figure 46 – Diffusion barrier effect on S11

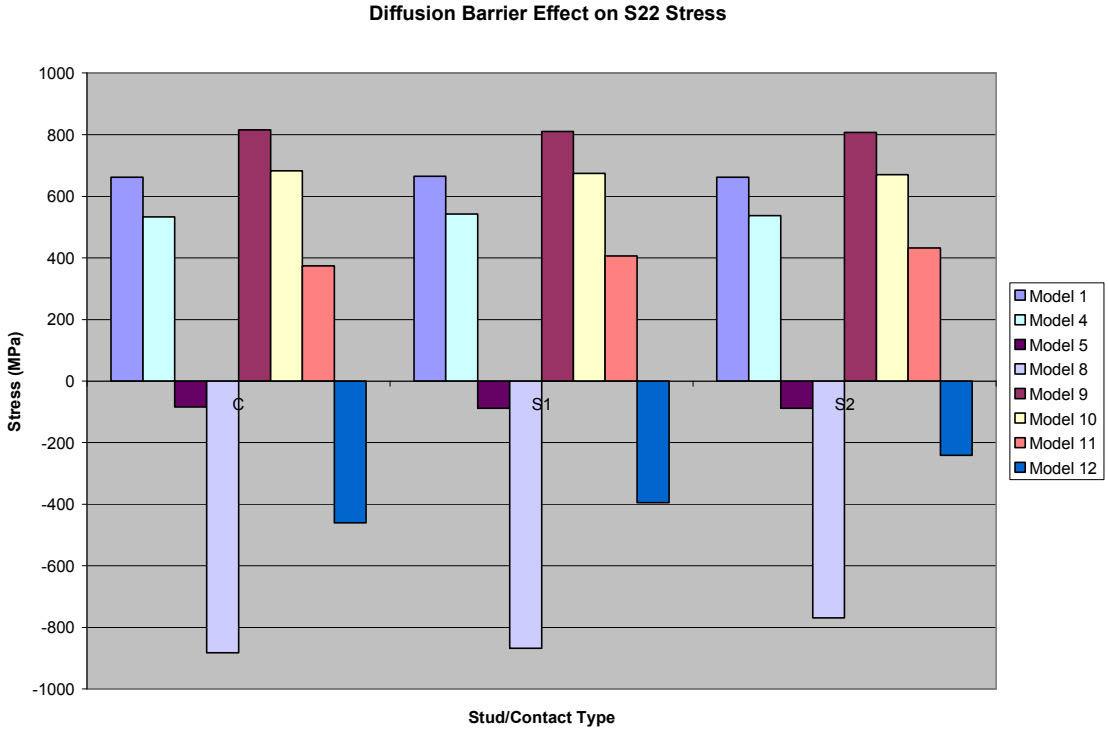

Figure 47 – Diffusion barrier effect on S22

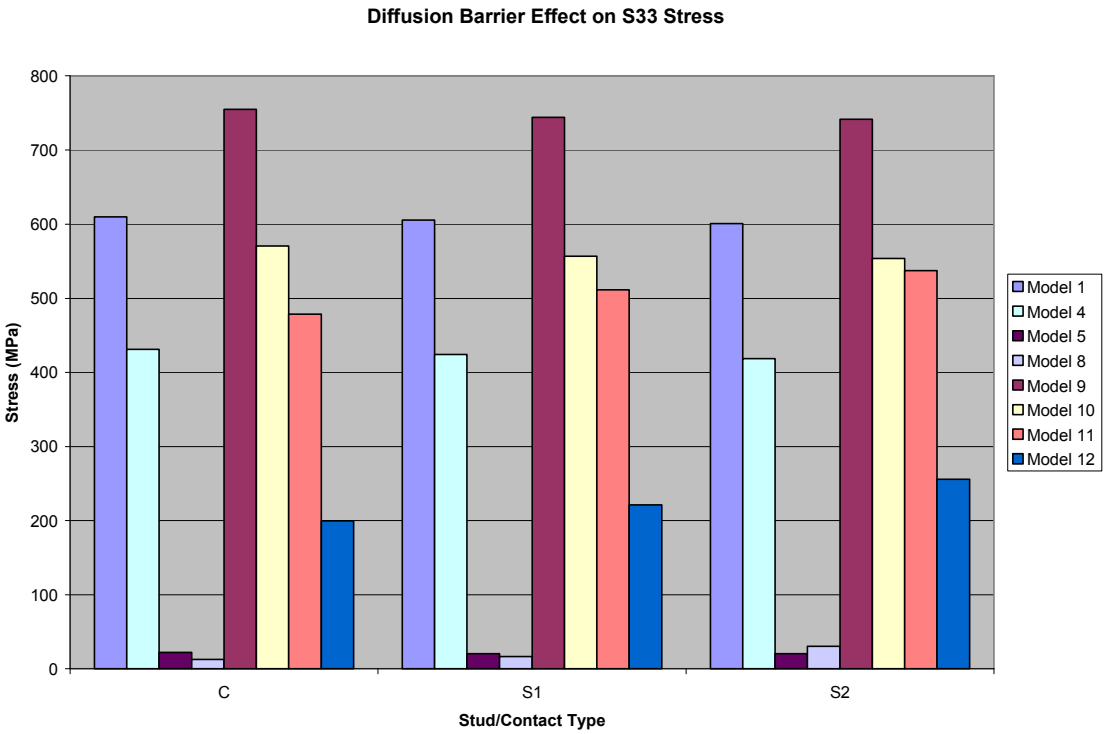

Figure 48 – Diffusion barrier effect on S33

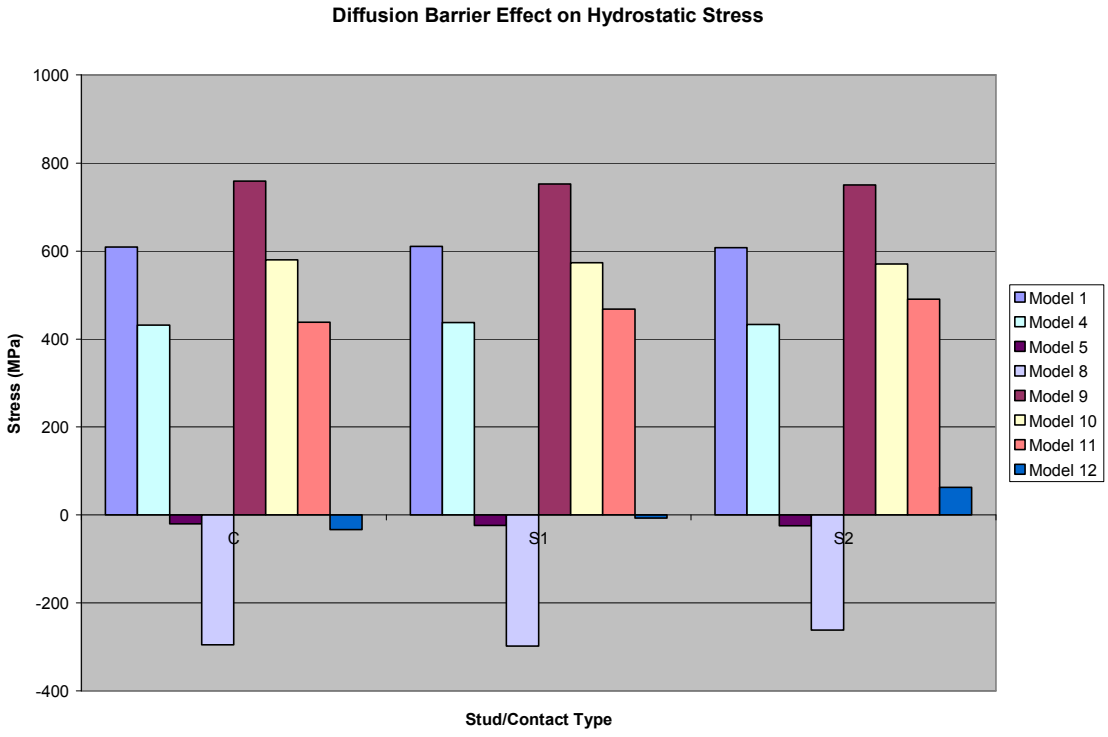

Figure 49– Diffusion barrier effect on Hydro

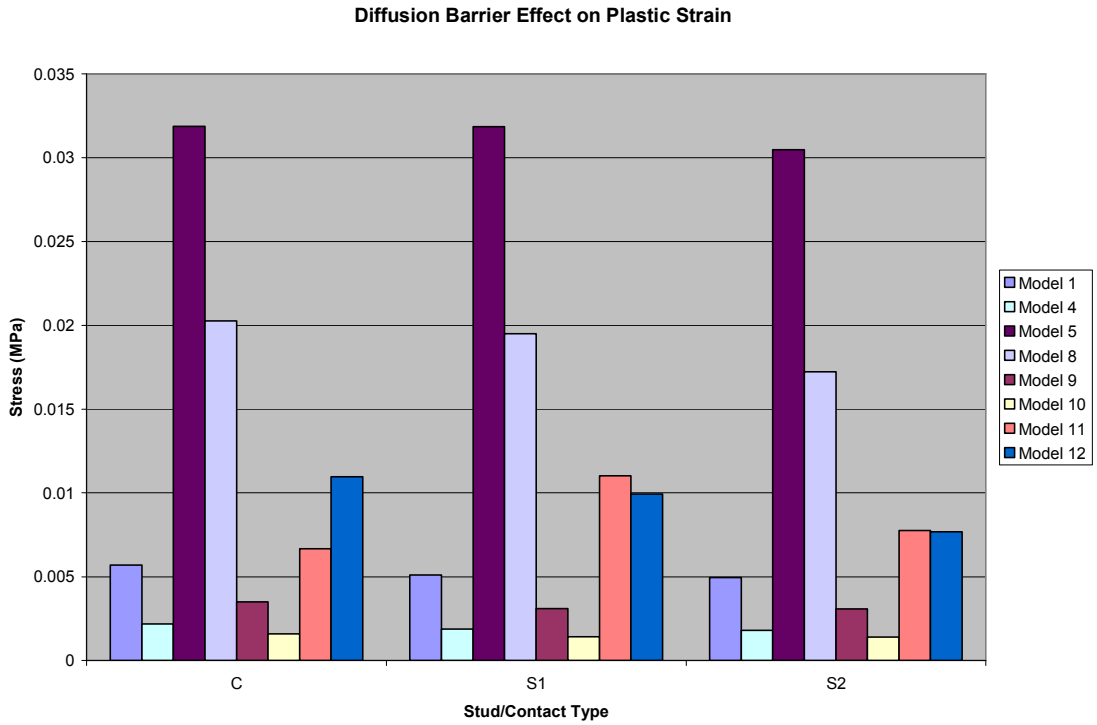

Figure 50– Diffusion barrier effect on Pemag

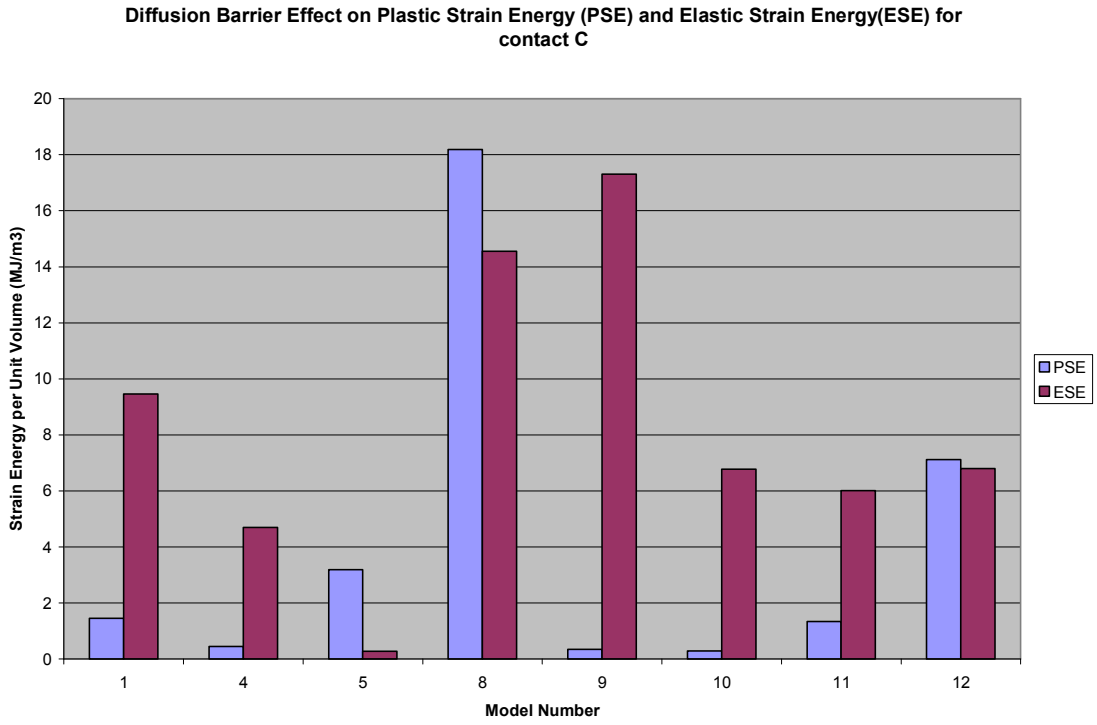

Figure 51– Diffusion barrier effect on PSE and ESE for contact C

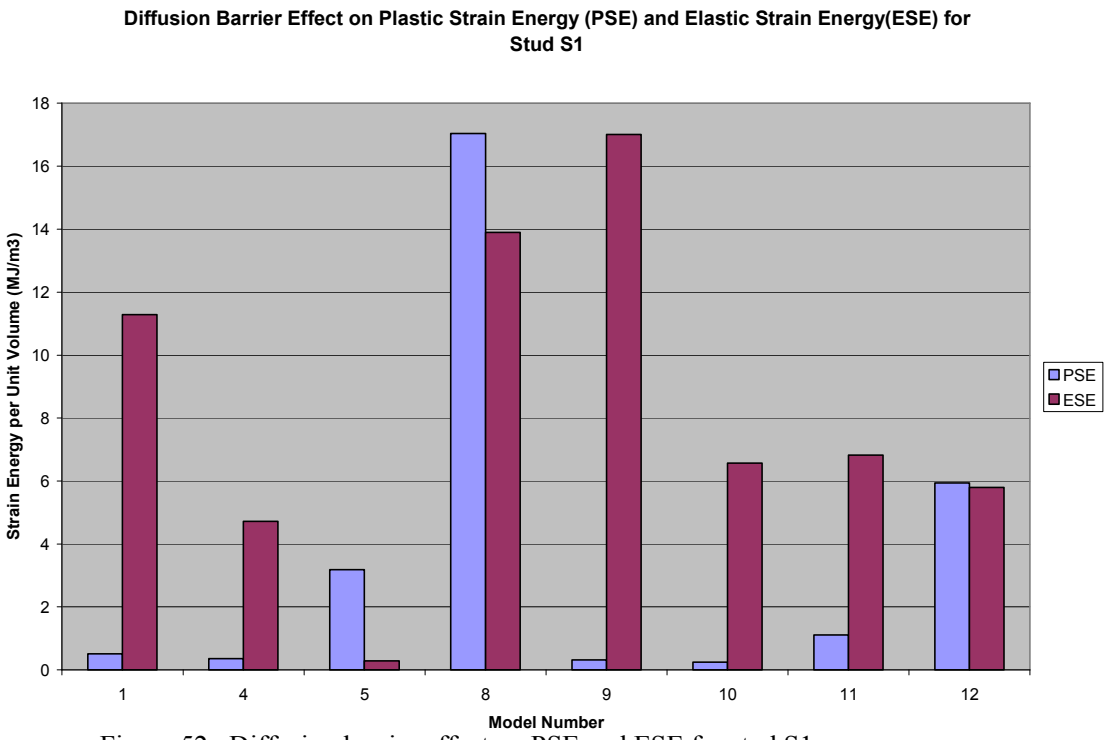

Figure 52– Diffusion barrier effect on PSE and ESE for stud S1

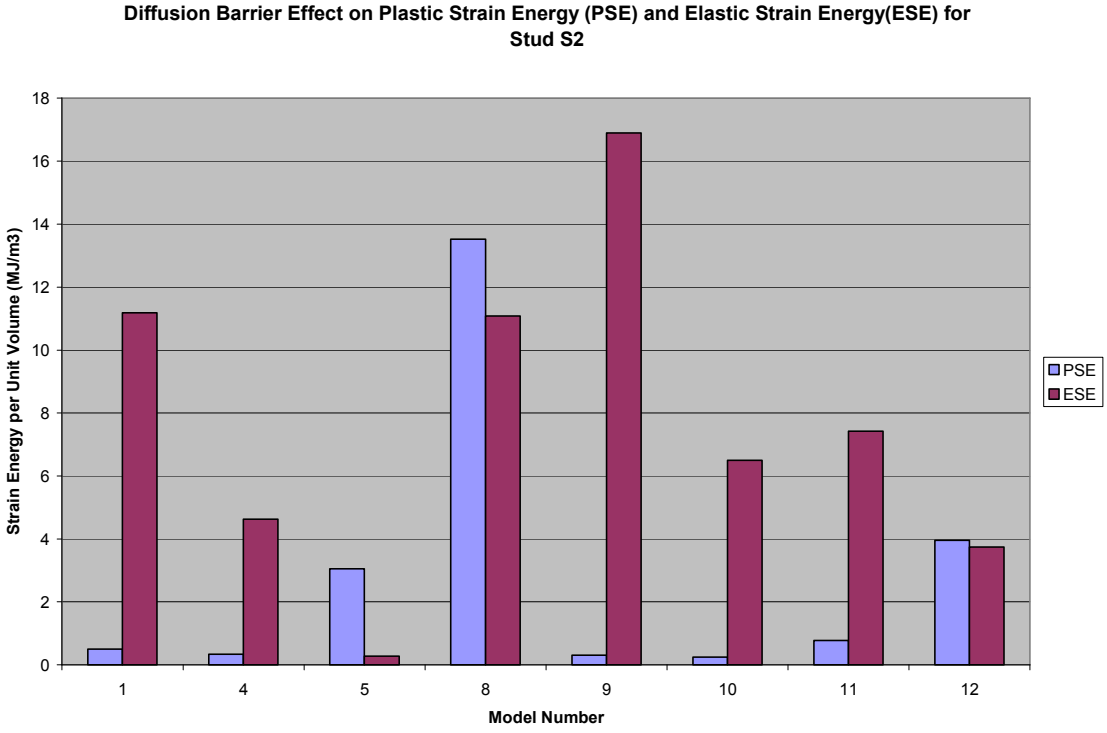

Figure 53– Diffusion barrier effect on PSE and ESE for stud S2

3.6 Discussion of results for sections 3.4 and 3.5

- The stresses in Al_3 were higher than that of Cu studs/contact when SiO_2 is used as a dielectric. The higher stresses in Al_3 were due to a higher thermal expansion mismatch between SiO_2 and Al_3 than that between Cu and SiO_2. Lower stresses are obtained if W studs are used due to even much lower thermal expansion mismatch between W and SiO_2. The best choice when SiO_2 is used is the combination of Al_3 interconnect with W stud due to lower tensile stresses (Figures 33-36)
- The usage of SiLK, a low dielectric material has the effect of reducing the high tensile stresses in Al_3 and Cu (see Figures 33-36) studs because SiLK permits more plastic deformation in Al_3 and Cu studs. Plastic deformation relaxes the stresses (see Figure 37)
- The stresses in Al_3 stud are lower than that of Cu when SiLK dielectric is used because of the higher thermal expansion mismatch between Cu and SiLK. The huge thermal expansion mismatch between W and SiLK and the absence of plastic deformation to relax the high stresses generated leads to very high compressive stresses in W(see Figures 34 and 33). The best choice when SiLK is used from the thermal stress point of view will be Al_3 interconnect and stud but this advantage might be offset from an electrical standpoint due to the higher electrical resistance of Al_3 compared with that of Cu
- SiLK reduces the problem of stress induced void formation in both Al_3 and Cu studs due to a lower tensile hydrostatic stress (see Figure 36) but increases propensity of the studs to fail by interfacial delamination due to high shear

stresses. The high shear effect was examined by calculating the volume average plastic strain energy (PSE) since it is shear stresses that are responsible for plastic flow. The plastic strain energy is then compared with that of the elastic strain energy (ESE). Interfacial delamination now becomes the reliability problem when Al_3 or Cu is used with low K dielectrics (see Figure 38-40) due to higher PSE relative to that of ESE. This trend was not the case with SiO_2. Similar results were obtained from both experimental and numerical results for Cu interconnects with low k dielectric [25-26]

- The inclusion of a TiN diffusion barrier in Al_3 and Cu studs increases the stresses and confines the stud by allowing less plastic deformation when both SiLK and SiO_2 dielectric are used as shown on Figures 46-50. The diffusion barrier TiN increases the propensity of void formation in Al_3 and Cu studs but reduces the problem of interfacial delamination. The propensity to fail by voiding is due to an increase in tensile hydrostatic stress when TiN is used. Despite the reduction in shear stresses and PSE when TiN is used with SiLK, Cu still exhibits a propensity to fail by interfacial (Figures 51-53). Similar trend was obtained experimentally and numerically for Cu interconnects with low k dielectric [25-26]. The diffusion barrier layer effect is more pronounced in the low-k dielectric. Its effect should not be neglected in low-k dielectrics as was done in previous analysis of studs in SiO_2 dielectric [8-9].
- The stress concentration or critical regions for S11, S22 and hydrostatic stresses when SiO_2 is used were the interface between the stud and the interconnects (regions **A** and **B** in Figures 41,42 and 44).The interface between the stud and

dielectric at the back of the stud (regions **C** and **D** as shown in Figures 41-44) were also critical regions for all stress components . Region **E** (plane of symmetry) also correlated with critical regions for stress S33. The stress concentrations regions correlated with the regions of low plastic deformation. The defective or critical sites obtained in this project were similar to those obtained experimentally and numerically for studs [2, 8]. The experimental defective sites correlated with regions of high concentration centers [8]

- The stress concentration or critical regions when SiLK dielectric was used was primarily the interface between the stud/dielectric at the back region of the stud (that is regions **C** and **D**) with critical regions **C** and **D** now extending to almost all the interface between stud/dielectric.

CHAPTER 4

SUMMARY AND CONCLUSIONS

The reliability of microelectronic circuitry depends greatly on the thermal stresses induced during typical integrated circuit fabrication. Failure mechanism in integrated circuit such as void formation, electro -migration and interfacial delamination are all induced by thermal stresses. The thermal induced stresses and plastic strain in studs/vias that connect metal interconnects to another in microelectronic circuitry was determined in this project with respect to changes in geometric parameters and material choice using an elasto-plastic three dimensional finite element method.

The thermal stresses (three normal stress and hydrostatic) in aluminum studs did not exhibit much dependence on the hardening exponent hence the assumption of perfectly plastic is good when considering thermal stresses in aluminum. The plastic strain shows a strong dependence on the hardening hence if plastic strain is of primary concern the perfectly plastic assumption is not sufficient. The stress exhibited a peak value at a stud aspect ratio of 2.5 beyond which the stress reduces at the expense of increasing plastic strain. The thermal stresses increases in studs as the spacing between the interconnect increases while the plastic strain reduces. The stress concentration regions (probable sites for void formation and interfacial delamination) were the stud/interconnect and the stud /dielectric interfaces. The inclusion of diffusion barrier layer such as TiN in studs will reduce the plastic deformation in Aluminum and Copper studs consequently leading to higher stresses in studs thereby increasing the propensity to fail by void formation .The barrier layer reduces the effect of interfacial delamination in

both low k and SiO_2 dielectrics. The diffusion barrier layer effect is more pronounced in low- k dielectric. Its effect must not be neglected as done in previous analysis of studs in SiO_2 dielectric. The drive in microelectronic circuitry towards Copper interconnects and studs with low k dielectric will shift the reliability concern in studs from stress induced void formation to interfacial delamination

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